

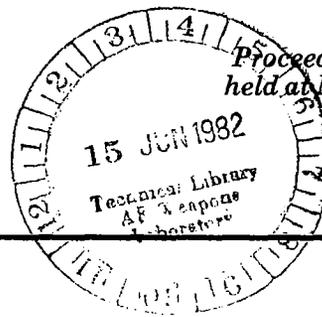
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Joint University Program for Air Transportation Research - 1981

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*Proceedings of a conference
held at NASA Headquarters
Washington, D.C.
December 11, 1981*

NASA



NASA Conference Publica

Joint University Program for Air Transportation Research - 1981

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December 11, 1981

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**Scientific and Technical
Information Branch**

PREFACE

The Joint University Program for Air Transportation Research is a coordinated set of three grants sponsored by NASA Langley Research Center, one each with Massachusetts Institute of Technology (NGL-22-009-640), Ohio University (NGR-36-009-017), and Princeton University (NGL-31-001-252), to support the training of students for the air transportation system. These grants, initiated in 1971, encourage the development of innovative curriculums and support the establishment of graduate and undergraduate research assistantships and internships.

An important feature of this program is the quarterly review, one held at each of the schools and the fourth at a NASA facility. This latter review for 1981 was conducted at NASA Headquarters in Washington, D.C., December 11, 1981. At these reviews the program participants, both graduate and undergraduate, have an opportunity to present their research activities to their peers, professors, and invited guests from government and industry.

This conference publication represents the second in a series of yearly summaries of the activities of the program. (The 1980 summary appears in NASA CP-2176.) The majority of the material is the efforts of the students supported by the grants. Because of the ongoing nature of some of the work, certain graphics (notably photographs) are not of high quality; however, it was decided to publish the best material available, and if the reader's interest is sufficient, the appropriate advisor can be contacted for more recent and complete data.

Three types of contributions are included. Completed works are represented by the full technical papers. Research previously published in the open literature, for example, theses or journal articles, is presented in an annotated bibliography. Status reports of ongoing research are represented by copies of viewgraphs augmented with a brief descriptive text.

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**Massachusetts
Institute
of
Technology**

INVESTIGATION OF AIR TRANSPORTATION TECHNOLOGY AT MASSACHUSETTS

INSTITUTE OF TECHNOLOGY, 1981

Professor Robert W. Simpson
Director, Flight Transportation Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139

SUMMARY OF RESEARCH

There have been three areas of research sponsored by the Joint University Program at MIT during the past year: 1) Dynamic Scheduling of Runway Operations at a Major Airport; 2) General Aviation Electronic Flight Displays - (P-POD); 3) Prevention of Airframe Icing with Microwaves. There are three faculty responsible for supervising student research in the program; Robert Simpson, Antonio Elias, and Walter Hollister.

1. DYNAMIC SCHEDULING OF RUNWAY OPERATIONS

In past years, an ATC simulation facility called TASIM (Terminal Area Simulation) was developed to provide a tool for investigating human factors problems associated with automated decision making in ATC. The current research goals are associated with demonstrating in real time the potential reductions in delay from the introduction of dynamic scheduling of landing and takeoff operations for a system of runways at a major airport. This potential was first indicated by Dear's research (ref. 1).

In the past year two decision-making modules have been designed. The "Traffic Scheduler" module has been successfully coded and tested in the Boston scenario for a single runway with landings and takeoffs. A schedule of runway operations is displayed on an auxiliary CTID (Controller Traffic Information Display), and can be seen to change dynamically as real time arrivals and departures enter the system. On the controller's "radar" display, the current FAA ARTS III display is augmented to show "boxes" for landing arrivals along the extended runway centerline. These landing boxes show the desired position of landing aircraft for its landing schedule. A second module "Flight Path Generation" has been designed but is not yet tested successfully. It generates a sequence of commands of altitude, heading, and speed for landing aircraft such that they will be vectored into their box. Further modules associated with conformance and hazard monitoring have yet to be designed, and the problems of man-machine interactions with this automated "decision support" software which arise from incorporating controller "override" capability (so that he remains in command of the computer system) and from operational problems (such as changing runways) have not yet been addressed. There is an annotated slide presentation by John Pararas in this publication.

2. GENERAL AVIATION ELECTRONIC FLIGHT DISPLAYS (P-POD)

This research is focused on the interface between the pilot and the display systems of his aircraft. We are interested in the information handling processes and consequent pilot workloads encountered in flying IFR in today's and future ATC systems. In the past year, a low cost digital electronic flight display has been assembled using microprocessor components commercially available to the home computer hobbyist. This display is called P-POD (Programmable Pilot-Oriented Display) and is described in a conference paper by Professor Antonio Elias. There are two research projects currently underway using P-POD. The first is described by James Littlefield in an annotated slide presentation given at the conference. Its goals are to create an operational "long range" RNAV display by interfacing P-POD to a commercially available Loran-C receiver. This will be tested on the bench, and in flight test. The second project has interfaced P-POD to a table-top general aviation cockpit simulator to create a novel electronic flight director display which provides rate of cross-track deviation to the general aviation pilot. The display has other proposed projects concerned with LNAV approaches to a runway and the development of an "Electronic Kneepad" for flight management activities of the IFR pilot. These are described briefly by Elias in his paper.

3. PREVENTION OF AIRFRAME ICING WITH MICROWAVES

John Hansman describes his research into the possibilities for using microwave energy to preheat supercooled water droplets before they reach an airfoil. This consists of some theoretical work on droplet movement and flattening due to accelerations due to the flow around the airfoil. The droplet shape is important in determining the optimal frequency for the microwave and whether there is sufficient time to heat the droplets at speeds typical of general aviation aircraft. There is also an experimental portion of the research in a rain-fog section of a 1 foot by 1 foot wind tunnel at MIT. This is aimed at a proof of principal experiment with a prototype system mounted on an airfoil section in the tunnel where measurements can be made of microwave power requirements and droplet temperatures.

REFERENCE

1. Dear, Roger D.: The Dynamic Scheduling of Aircraft in the Near Terminal Area. Flight Transportation Report R76-9, Dept. of Aeronautics and Astronautics, Massachusetts Institute of Technology, Cambridge, Mass., Sept. 1976.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

ANNOTATED BIBLIOGRAPHY, 1980-81

Pararas, John: Man Vehicle Systems Research Facility: Functional Specification of the ATC Subsystem. Flight Transportation Laboratory Report R80-13, Department of Aeronautics and Astronautics, MIT, December 1980.

This document establishes the functional and operational specifications for the ATC subsystem of the Manned Vehicle Systems Research Facility to be built at NASA Ames Research Center. The ATC subsystem will provide a realistic ATC environment for two transport cockpit simulators. Fuel mission, high fidelity simulation of extended flights in both today's and future ATC systems is required. The ATC subsystem design recommended consists of three audio/visual controller stations and a corresponding three pseudo-pilot stations with a voice disguiser capable of representing several different pilot voices. The ATC subsystem makes use of software developed for TASIM under the Joint University Program.

Natarajan, Krishman: Use of Loran-C for General Aviation Aircraft Navigation. Flight Transportation Laboratory Report R81-2, February 1981.

This report describes an extensive evaluation of Loran-C for use by general aviation. Flight, ground, and antenna tests were done. Flight tests measured the accuracy and the ability to make approaches. Receiver reliability and susceptibility to atmospheric noise were also studied. Ground tests looked into grid stability and grid warpage. Antenna tests were done to evaluate three antenna configurations -- ADF, vertical whip, and trailing wire antennas.

The measured accuracy met FAA AC 90-45A requirements for all phases of flight. Loran-C was found to be satisfactory for approaches with AC 90-45A specifications. Reliability was 99.7%, and the receiver was insensitive to atmospheric noise. The time difference grid was stable in the long run. Antenna tests showed the ADF and vertical whip antennas to be suitable for airborne use.

It is concluded that Loran-C is suitable for navigation as an alternative to VHF RNAV. This navigation system is suitable for use in general aviation aircraft.

DYNAMIC SCHEDULING
OF RUNWAY OPERATIONS

John Pararas
MIT, Flight Transportation Laboratory

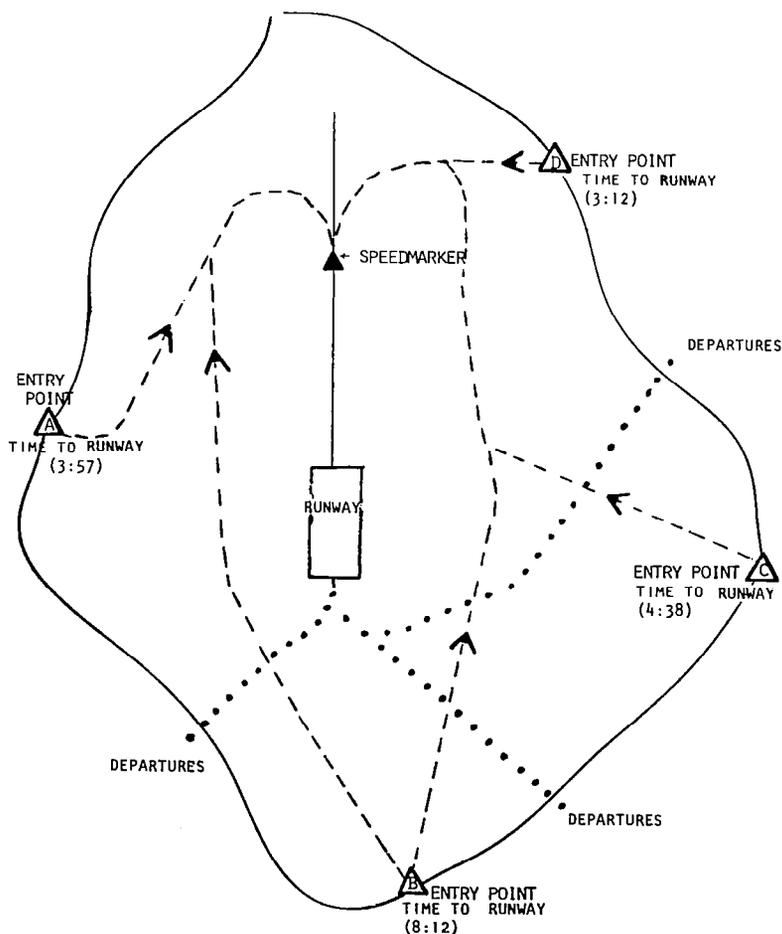
RESEARCH OBJECTIVES

- Demonstrate the feasibility of automated ATM/C decision making in the terminal area
 - Develop prototype algorithms for automation functions
 - Runway Scheduling
 - Flight Plan Generator

Terminal Area Geometry

Due to the airway structure of the enroute airspace, landing aircraft tend to enter the terminal area airspace at specific points called entry fixes. Nominal approach routes (the dashed lines) define typical paths leading from the entry fixes to the runway threshold(s). Similarly, nominal departure routes (dotted lines) define typical paths for departing aircraft.

Whenever a new arrival enters the terminal area, its preferred time of arrival at the runway is estimated based on the entry fix and the associated nominal approach path. For departures the preferred time of arrival at the runway is determined using an estimate of the taxiing time. The nominal sequence of operations at the runway is determined based on the preferred times of arrival at the runway of all aircraft currently in the system. This sequence is perturbed to optimize the runway utilization for the given traffic, thus producing the optimal schedule of operations. Given the latter, 4-dimensional flight plans are generated for all aircraft.

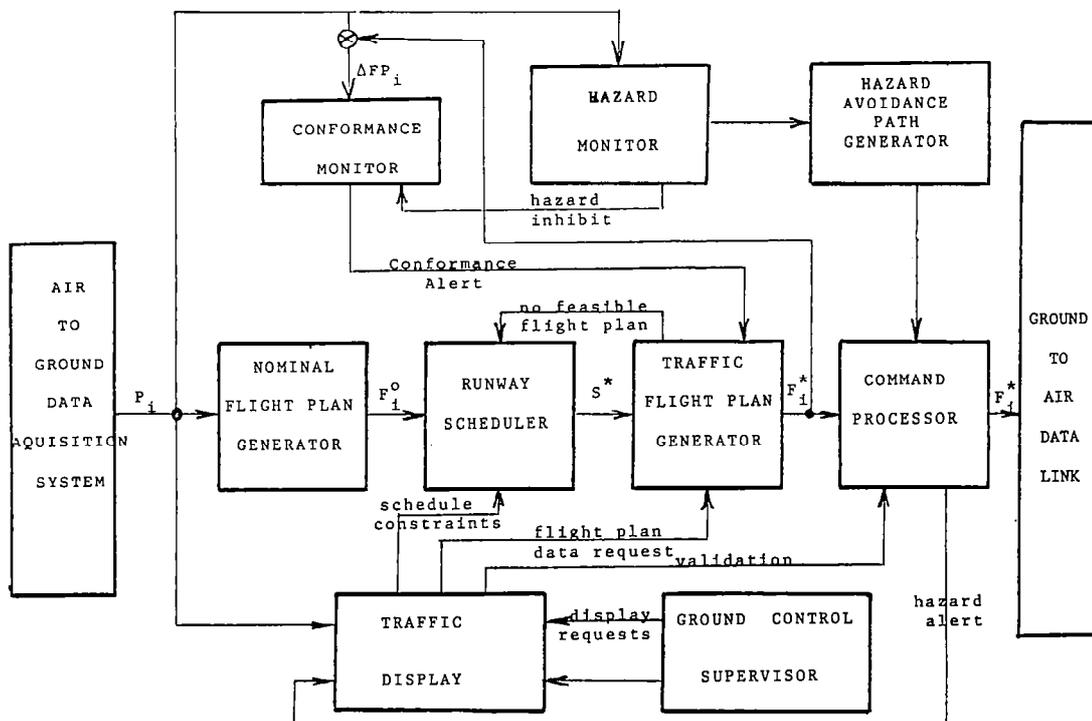


Schematic Diagram of the Terminal Area ATM/C System

The air-to-ground data acquisition (surveillance) system provides position information on all aircraft in the system. Nominal flight plans are generated for new entries and provided to the runway scheduler which updates the optimal schedule of operations at the runway(s). The traffic flight plan generator updates the flight plans according to the new schedule. The decision process is now complete until a new aircraft enters the system.

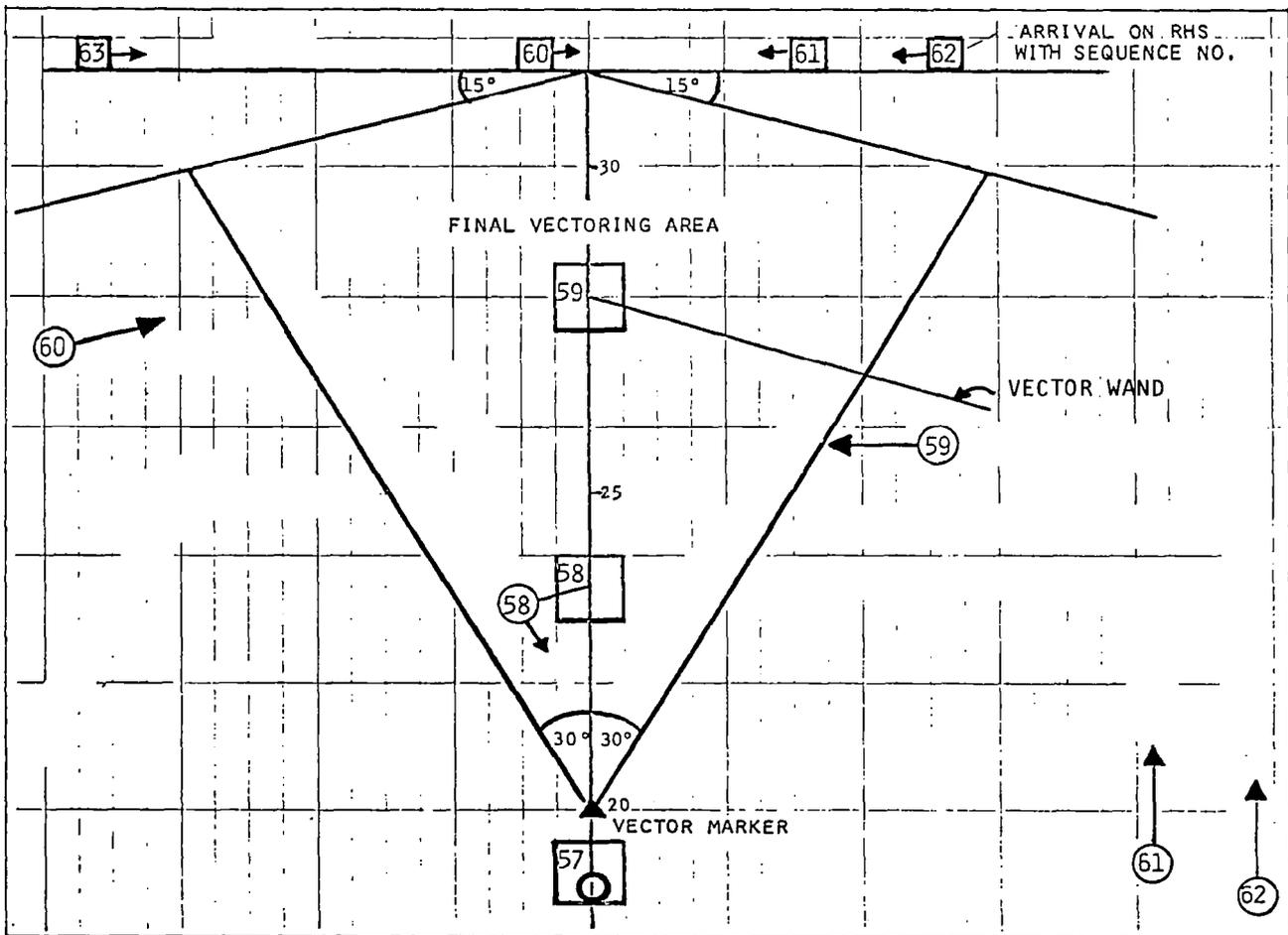
The command processor is responsible for the timely dispatch of commands to the air traffic controller. This is done through the traffic display. The commands can also be transferred directly to the pilot via an air-to-ground digital data link if one is available. The commands are such that will keep the aircraft in conformance with their flight plans. The traffic display provides the controller with a situation display of all the traffic in the system and allows him to communicate with the remaining system through "display requests".

The conformance monitor compares actual and desired aircraft positions and generates an alert when the discrepancy detected exceeds prespecified limits for some aircraft. This in general will cause a new flight plan to be generated for this (and possibly other) aircraft. The hazard monitor compares separations of short term projections of aircraft positions and generates an alert when violations of ATC separations are imminent. Again such an alert will require new flight plans to be generated but first avoidance paths are generated for the aircraft in hazard.



Final Vector Controller Display

This display is designed to facilitate precise delivery of landing aircraft at the outer marker without automated flight plan and command generation. Each box corresponds to the landing aircraft having the same number in the landing sequence. The boxes are moving along the runway centerline extension at the landing speed of the corresponding aircraft. The distance from the threshold is such that the aircraft reaches the runway at its scheduled landing time. Given the current and the landing speeds of the aircraft we can determine the relative bearing between the aircraft and its box such that if the aircraft then turns to intercept the ILS it will intercept the box before it reaches the outer marker. The wands shown are the pictorial representation of the appropriate relative bearing. The controller needs to approximately time the aircraft so that it will be within the final vectoring area when it is touched by the wand of its box. At that time the turn to intercept the ILS should be given.



Tri-University Conference

Accomplishments to Date

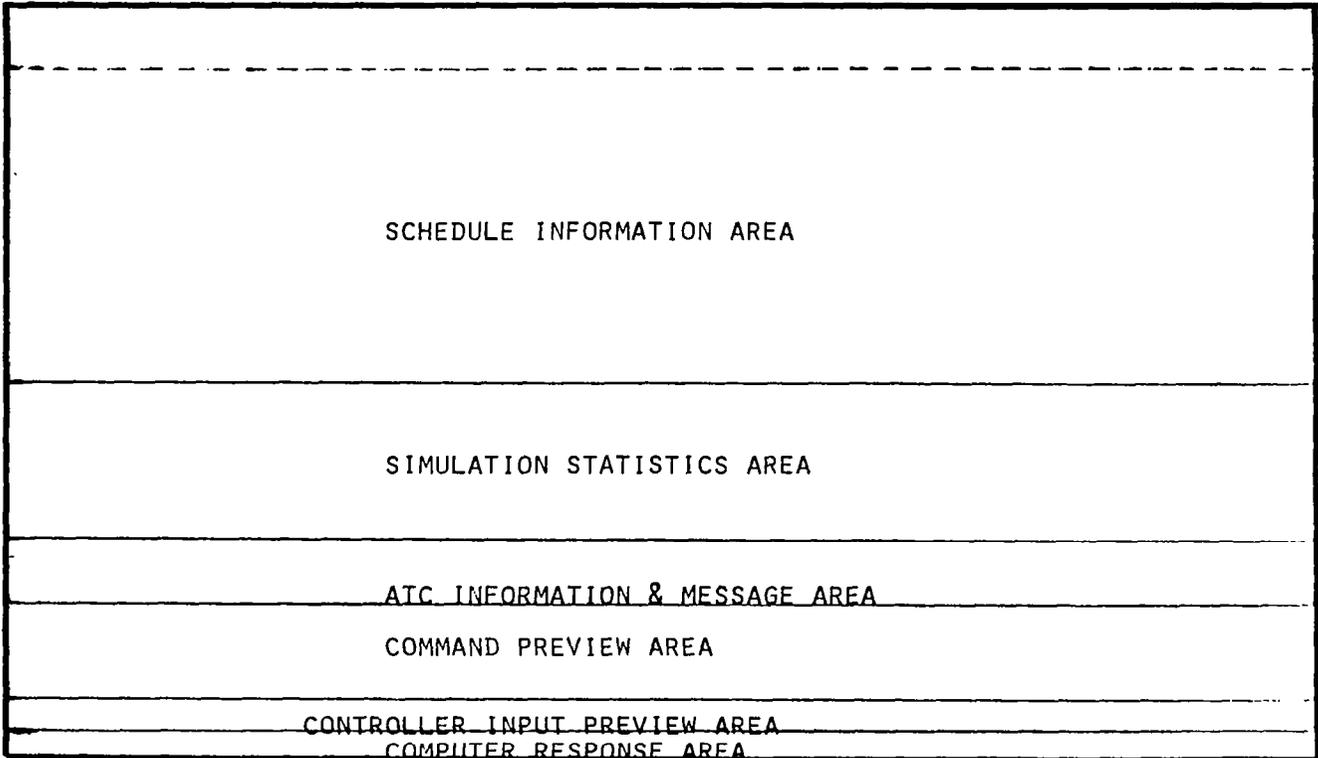
A major portion of the work has been consumed in creating TASIM (Terminal Area Simulation). It is a flexible research simulator for ATC problems involving automated decision making for ATC, but can be useful to many researchers interested in ATC problems. It forms the basis for the ATC subsystem to be built for the MVRSF (Manned Vehicle Research Simulation Facility) at NASA Ames Research Center, and is of interest to the FAA Technical Center at Atlantic City.

At present the simulation can be operated by a human controller through the keyboard in a scenario of the Boston Logan terminal area. The automated runway scheduler based on the CPS (Constrained Position Shifting) method of Dear has been coded and operates successfully with the display scheme shown for the Final Vectoring. The automated Flight Plan generator has been designed but is not yet operational. The Command Processor is operational and passes controller-generated commands directly to each target aircraft. There are two controller displays. The ATC or PVD display is a reproduction of the current ARTS III display (with the Final Vectoring display augmentation). There is also an auxiliary CTID (Controller Traffic Information Display) which displays the dynamically changing schedule for runway operations, some simulation statistics, and has message areas, command preview areas, etc., for controller interaction.

1. TASIM INTERACTIVE SIMULATION

2. SOFTWARE

- RUNWAY SCHEDULER
 - CPS
- TRAFFIC PLAN GENERATOR
 - TERMINAL AREA NETWORK
 - design of the algorithm
- COMMAND PROCESSOR
 - CONTROLLER INPUTS
 - TRAFFIC PLAN GENERATOR INPUTS
- DISPLAYS
 - ATC DISPLAY (PVD)
 - CTID



CONTROLLER TABULAR INFORMATION DISPLAY
(CTID)

PPOD PROGRAMMABLE PILOT-ORIENTED DISPLAY

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SUMMARY

A general-purpose low cost research microprocessor system for General Aviation has been developed at MIT under the sponsorship of the Joint University Program. This system is intended to be the vehicle for individual research efforts in low cost airborne hardware and software as well as advanced microprocessor based navigation systems and techniques. During 1981, two such research projects were undertaken, yielding results in the areas of micro hardware/software design, cost and performance, and pilot/computer interface. Five new projects are being developed for 1982, including a new approach to low-cost flight software reliability and a time-difference based Loran approach procedure that eliminates the need for propagation corrections and latitude/longitude transformations.

INTRODUCTION

Before the advent of microprocessors, the design of navigation systems was strongly influenced by the lack of convenient computational capabilities. This lack, combined with the need to minimize pilot workload, led to "direct readout" systems such as VOR/DME, where the signal scheme itself directly yields navigation information in easy to use format, e.g. rho-theta. Similarly, systems which required any significant amount of "post-processing", such as Loran, were deemed unsuitable for aeronautical use, unless a crewmember was dedicated to the navigation task.

Microprocessors make available so much computational capability that this traditional limitation no longer exists, thus opening up important new possibilities in the design and use of avionic systems. However, this technology has evolved in such a way that the principal costs involved in the use of microprocessors in avionic systems are not the cost of the processors itself, but of the environment required to support the digital processing functions, namely:

- 1) The development (non-recurring) cost of flight software
- 2) The certification of the digital hardware and software (also non-recurring)
- 3) Repetitive design of the discrete (i.e. non-LSI) hardware, e.g. busses, cards, interfaces, etc. (mainly a recurrent cost)

These high non-recurrent and recurrent costs appear to have driven the avionics industry to a very specific technological and marketing niche, namely the high cost, high performance devices used on executive aircraft. Thus we find units such as the Garrett AirResearch 2000 navigator, with both high performance and high price. Ironically, most of these aircraft operate with two crewmembers so that, in spite of the increased complexity of the aircraft, the resulting workload may be lower than the typical single-pilot IFR situation on a simpler but less equipped aircraft. It is precisely this situation that could benefit the most from workload-reducing microprocessor based avionics.

If this segment of the General Aviation community is to receive the benefits of microprocessor-based systems, ways must be found to make the low-cost market attractive to industry. The first step is to demonstrate that microprocessor avionics can be produced at a low unit cost without the risk of committing to very large production runs. Only after this has been demonstrated is industry likely to embark on larger production run projects with larger non-recurrent costs.

We believe that there may be major cost-reduction demonstration opportunities on each of the cost areas mentioned before, in particular:

- 1) Improved software techniques, which may reduce both the development and the certification costs of embedded software
- 2) The use of standard ("off the shelf") modules for commonly-used functions, such as power supply, data busses, interfaces, memory, processors systems, display drivers, etc.
- 3) Multifunctionality; that is, the use of a single digital processor to perform a number of avionic functions, rather than embedding individual microprocessors on each avionics box (1)

(1) Distributed processing, that is, the use of individual processors for each function, may be the best design when other factors, such as performance and reliability, dominate over cost.

OVERVIEW OF PPOD PROJECT

The motivation for developing PPOD was to make available to researchers a low-cost general-purpose tool with which to investigate the areas mentioned above. The result is a three-processor system (main, I/O, display) using standard hardware and software, which can be configured (both from the hardware and the software point of view) for a wide range of operations and uses. The intent is that individual research projects be undertaken using this system, in order to try out novel digital avionics ideas while at the same time accumulating the experience of using and developing low-cost hardware and software.

The PPOD hardware consists of an S-100 box (including the motherboard and ground power supply), a single-board Z-80 processor (including serial I/O, disk controller and EPROM burner), 64K of dynamic memory, 32K of ROM space, a high-resolution monochrome raster display (using its own Z-80), and a slave processor (also a Z-80) with DMA capability, 24 bits of parallel I/O and small amounts of RAM and ROM.

The emphasis of all of these sub-projects will be the reduction of single-pilot IFR workload, with the secondary goal of reducing the physical complexity of cockpit instrumentation.

SPECIFIC RESEARCH ISSUES: SOFTWARE

Although ultimately it will be up to industry to develop the actual designs for low-cost microprocessor based avionics, some of the research that may demonstrate the viability of doing so may be best carried out from the detachment of a non-commercial research organization, such as NASA or the Universities; in commercial avionics development, marketing and timing reasons may prevent the kind of general-application research that PPOD is intended to support.

In the software areas, three specific issues are addressed:

- 1) The use of high-order languages
- 2) The use of resident-based (as opposed to host-based) development systems
- 3) The development of standard software functions

Use of high-order languages

Large-scale aerospace processors, such as the IBM AP101, have modern high-order language support (e.g. HAL), whereas microprocessor flight software is commonly done in assembler code. One of the reasons for this situation is the large investment required to develop a high-order language environment (up to \$1M for the HAL system).

On the other hand, the explosion of the personal computer market has resulted in the development of a number of modern high-order language systems (Pascal, PL1, Forth, C, etc.) for microprocessors. Naturally but unfortunately, most of them are geared towards non-real time applications, and require disk drives for program operation. We would like to identify exactly the shortcomings of these systems, and what has to be added or modified to make them suitable for flight software use.

Finally, we would like to quantify the cost benefits of high-order languages in the GA avionics environment, in particular the tradeoffs between the reduction in software cost, the increase in memory needs, and the reduction in processing efficiency for significantly different languages and systems.

Alternative development systems

There are three possible approaches to developing microprocessor software, listed here in order of increasing procurement cost:

- 1) The use of an existing time-sharing system to edit, compile, link and, under certain circumstances, execute (by simulation) the flight code, or, alternatively, download it to the target machine for execution and checkout
- 2) The use of the target microprocessor itself both for development and checkout
- 3) The use of a specially-configured micro or minicomputer system geared towards software development (a "Development System")

Traditionally, embedded microprocessor software has been developed by the first and last methods, sometimes in combination. Use of the target machine for software development is another technique that has come of age with the explosion of the

personal computer industry. Each of the methods has advantages and disadvantages; with PPOD, we can experiment with the first two methods (the use of a Development System being beyond the reasonable reach of the project's budgetary expectations).

Standard software libraries

The last software research issue addressed is the use of standard functions in flight software, that is, the identification of functions that are general enough, and common enough so as to warrant the development of "library" modules to reduce subsequent software development/certification costs. Of particular interest is the human interface/display area, where a standardization of protocols and/or formats could also result in uniform user procedures across different designs.

SPECIFIC RESEARCH ISSUES: HARDWARE

In the hardware side, we will identify the hardware functions that are required, and relate these functions with board-level modules that are either currently available, or should be made available as "off the shelf" components for GA avionics use.

It should be noted that the purpose is not to determine the suitability or unsuitability of existing components for GA avionics use, but rather to identify the functions required, and to quantify the benefits that would accrue from the availability of such standard components. As a consequence of this research, we hope to identify opportunities for GA-oriented industry standards for busses, hardware interfaces, etc. that could be an incentive for production of standard boards.

Finally, in the systems design area, we hope to identify and quantify the acquisition, maintenance, and operating cost reductions that would accrue from integrating, rather than distributing, the processing functions.

Status of project

As of December 1981, the following milestones had been achieved:

- 1) A hardware configuration was selected, procured and assembled.
- 2) The hardware has been interfaced with a ground-based simulator for testing and development purposes.
- 3) An operating system environment for the various high-order languages has been selected and procured, including elements of a resident software development system (e.g. compilers, assembler, linker, full-screen editor, etc.)
- 4) The first high-order language system (PL1) has been procured.
- 5) Two pilot projects have been started, and are yielding initial research results.

Hardware configuration

The "S-100" family of hardware components was selected for P-POD; the main basis for this selection was the large number of board-level components available for this family, including processors, memory, device controllers and I/O, ROM, video displays, voice I/O, etc. The bus used in this family (and from which the name derives) is not without its faults, particularly in the area of noise immunity, bandwidth, and signal path architecture. On the other hand, it is a flexible design whose noise performance has been improved with active termination and heavy-duty construction, and whose signal definition faults have been at least partially remedied by an IEEE standard definition (IEEE 696) of the bus.

The initial configuration consisted of a Teletek FDC-1 single-board processor, a Measurement Systems and Controls (MSC) 64K dynamic memory board, a Digital Research Computers 32K selectable-address ROM board, and a Scion Corp. Microangelo display board.

The FDC-1 board includes, in addition to the Z-80 chip, two serial ports, floppy controller, 2K of ROM, and an EPROM burner. This board is used both for software development (using the CP/M floppy-based operating system) and for actual execution of the flight code. The Microangelo display board is a medium-resolution (512x480) monochrome bit-mapped raster display with a dedicated Z-80 processor, 8K of ROM and 2K of RAM (in addition to the screen RAM). Communication between the main processor board and the display board is by buffered interrupt driven physical I/O.

Earlier into the first project (Loran-C pilot interface) it was determined that the amount of I/O that could be accomplished by the main processor board was limited, and therefore a Teletek I2 board was procured. This board, which is produced commercially as an Intelligent Interface for devices such as Winchester hard disks (and therefore geared towards the OEM market), consists of a Z-80 processor, 2K of RAM, 2K of ROM, and the bus support circuitry required to interface with the bus owner (the Z-80 on the FDC-1) by a combination of vectored interrupts and Direct Memory Access.

These boards are contained in a California Computer Systems motherboard and card cage, which includes an unregulated heavy-duty 115 volts power supply to feed the series regulators on each of the boards. For flight use, the power supply is fed AC from a 300 watt static inverter.

PROJECT #1: VOR/RNAV-LIKE INTERFACE FOR LORAN-C

The first project initiated under P-POD was a display system that would allow a pilot to use a Loran-C receiver as a rho-theta navigation device similar to a VORDME/RNAV system. The motivation for this project was the observation that pilots prefer the rho-theta presentation of information to almost any other type of presentation, including maps. Whether this preference is due to the considerable experience that pilots have with the VOR system, or whether the popularity of the VOR system is due to its rho-theta presentation, is subject for debate.

In any case, the advantages of Loran (low equipment cost, wide area coverage) could be combined with the ease of use of VORDME by a device that would store names and geographical locations of VORTAC's. The aircraft latitude and longitude, as determined by Loran, is then converted to great-circle bearing and distance to a VORTAC selected by the pilot, and presented in a form vaguely resembling the familiar CDI and DME range window. In addition, the system allows the pilot to define (in-flight or before the flight) waypoints using either latitude and longitude or offsets from existing waypoints, and to assign three-letter identifiers to these new waypoints.

To test this concept, P-POD was interfaced to an existing commercial receiver (a Digital Marine Northstar 6000). However, one of the factors that was considered in selecting this as the first P-POD project was the expected availability of low-cost Loran-C receiver boards, such as the Ohio University unit. The display produced, the definitions of the navigation terms used,

and the commands available to the user are summarized in Figures 1, 2 and 3.

The system has been tested both on the bench and on a moving vehicle. Flight tests during late summer of 1981 were hampered by power supply and antenna problems. Flight tests with a new DC power supply, retractable downwards-pointing whip antenna, and improved keyboard will begin this spring. A preliminary result of some interest is the figures for utilization of high-order language (PL1) versus assembler code, summarized in Figure 4. In essence, it is estimated that the use of PL1 reduced programming time by a factor of 7 (1000 lines of code vs. 7000 lines of code), while the program memory required increased by 40% (14,000 bytes vs. 10,000 bytes).

Of some concern is the total amount of memory used by the applications code (some 7700 bytes), considering that the total address space of these machines is only 64K bytes, and that the operating system takes some 6500 bytes out of them. On the other hand, one-third of this code is made up of pilot input handling and display routines that could be shared by other functions. Also, the system incorporates a large number of "features" not all of which may be considered "indispensable".

A major obstacle encountered during development of this code was that the PL1 system subroutines do not initialize storage memory, because they expect its contents to be initialized from diskette as part of the program load. When the code is resident in ROM, however, there is no program load, and thus no initialization of storage memory. A system was developed to simulate this function at a cost of 25% of the storage memory required by systems programs (application programs were coded so that they perform their own initialization). In spite of this fix, it was concluded that any high-order language system that is to be useful for GA avionics use must either explicitly initialize memory storage itself, or at least separate storage memory into two areas, one of which requires initialization and thus must be "replicated" in ROM.

Code for this project was developed both with the resident system and the time-sharing system. On the basis of this experience we conclude that:

- 1) The resident system is superior to the time-sharing system for developing I/O (including user interface and display) code, and for final code integration, due to its "closeness" to the target machine.

- 2) The time-sharing system can be extremely useful for development and coding of algorithm-intensive functions (i.e. math-intensive), due to its faster compilation turnaround and its more powerful mathematical debugging capabilities (debugging can be performed at the PL1 level).
- 3) The time-sharing system is superior for maintaining and preprocessing data bases (e.g. VORTAC identifiers and positions).

PROJECT #2: RATE-ESTIMATING ILS DISPLAY

Flight Directors are devices that combine navigation and attitude information (including rate information) and generate an attitude command that is displayed on the same instrument that displays attitude. By suitable generation of the command attitude, the pilot workload required to fly a high-performance aircraft (requiring substantial command lead compensation) can be greatly reduced.

On the other hand, Flight Directors are expensive devices, because they require attitude and attitude rate (and, sometimes, control surfaces position) information, and because the computation and display devices are electromechanical in nature.

General aviation aircraft usually exhibit benign dynamics⁽¹⁾ which make full Flight Directors somewhat of an unnecessary luxury. The dynamics of lateral control during ILS precision approaches, however, do involve a significant amount of pilot workload due to the piloting strategy required by the low-gain, low rate information localizer display. The data processing and display capabilities of a P-POD like device in the cockpit could be used to generate a rate-aided display, maybe not as sophisticated as a Flight Director, but at essentially zero marginal cost given the ILS receiver and the P-POD display.

For that cost to be indeed "zero", the display must not require the attitude and attitude rate data (and the corresponding

(1) Under the sponsorship of this same NASA Joint University Program, Princeton is examining the dynamic and handling features of GA aircraft that make them more or less suitable for single-pilot IFR.

electro-mechanical instruments) that the true Flight Director requires.(1)

This project attempts to produce a simple display, using ILS localizer information and digital filtering techniques to estimate lateral deviation rate. This rate information is then presented to the pilot in the form of a rotating CDI needle, very much like the one used in the Loran-C display.

The specific research issues addressed by this project are:

- 1) Adequacy of 8-bit processor throughput for fast repetition rate processes
- 2) Adequacy of bit-mapped displays for fast update rate control oriented (as opposed to navigation oriented) displays
- 3) Adaptability of interface subroutines developed for one project (Loran-C) for other projects

This project was developed and tested using a desktop simulator (ATC-610) of a Piper Cherokee Arrow single-engine retractable. A PDP-11/10 was used to extract simulator X-Y position and synthesize ILS localizer information from it. This localizer "signal" was then fed to P-POD, which then generated the display. Flight tests will begin as soon as a navigation receiver is procured for this purpose.

One of the results obtained so far is that bit-mapped displays, such as the one used by P-POD, complicate the display design process because they "erase" the background over which a symbol is written, unless special precautions are taken to "save" the background information. In essence, three approaches are possible:

- 1) Design the display itself so that symbols do not overlap; this was the approach taken on the Loran-C display. In the case of the Localizer, this led to awkward displays.
- 2) Save the pixels that are over-written by a symbol and restore them at the time the symbol is erased

(1) At most, a low cost single axis fluidic rate gyro may be required.

for re-positioning. This requires complex graphics primitives and additional memory.

- 3) Write the moving symbols by complementing, rather than 1-ing the pixels; erase the symbol by re-complementing, thus restoring the background symbol. Does not require complex code or memory, but two overlapping symbols have blank pixels at their common locations.

All three techniques will be explored during the coming year.

PROPOSED NEW PROJECTS

A number of projects, all using the P-POD hardware and software, and all contributing towards the ultimate goal of identifying cost-reducing techniques, have been identified and will be started as resources become available. Some of these projects are:

- 1) The possible use of redundancy to improve the cost/reliability ratio of flight software ("Layered-redundant coding")
- 2) A Loran-C non-precision approach procedure based on Time Differences, not on latitude and longitude of runways
- 3) An "electronic kneepad" that would make available flight information to the pilot in a dynamic fashion, as well as perform flight-plan following computations (using pilot inputs, not direct navigation information)
- 4) An R/Nav device using a single, digitally-tunable, fast-locking DME and a large VORTAC position/frequency catalog to achieve country wide "hands-off" navigation
- 5) The use of voice I/O to augment/supplement the above functions

The first two projects require some elaboration:

There are two approaches to reliability in avionics hardware: producing hardware that is essentially very reliable, and using

less reliable hardware in redundant numbers, with the appropriate error detection and correction protocols. Two excellent examples of these approaches are the Apollo Guidance Computer, a single unit with MTBF's in excess of 20,000 hrs, and the Shuttle Orbiter Main Computer Complex, using four identical units with MTBF's of less than 1000 hours. Economic considerations dictate which approach is the most cost-effective for a particular situation.

Software reliability can only be achieved by the first (or "brute force") method, since two copies of the same software are guaranteed to have the same identical bugs; as opposed to hardware, there is no distinction between the design and the fabrication stages, and thus there are no advantages to redundant copies of the same code.

If, however, identical functional specifications for software are given to different software designers (i.e. coders), then there will be no correlation between the bugs in one version of the software and another. Such "truly redundant" software then has to be executed in an environment that recognizes differences in their outputs, and takes appropriate action in case of disagreement, much in the same way as redundant hardware.

The cost of producing two independent codes for the same function is, indeed, twice that of producing a single version.(1) However, that cost may very well be much less than that of testing and inspecting the single version to achieve the same degree of confidence that would result from the redundant execution. Also, any deficiencies in the specifications themselves will show up on both versions, requiring either duplicate specifications (hence the term "layered software redundancy"), or the use of conventional brute force reliability techniques for all higher level software and specifications.

To our knowledge, this approach has never been tried. In order to evaluate its potential, an experience base must be developed, including cost and performance statistics. We propose to use the P-POD project, and the sub-projects developed under it, as a test bench for the redundant coding concept. Selected functions will be double-coded by different individuals (using different languages, if possible) from the same specifications. The Operating System environment will be modified to handle the double-calling of the subroutines, comparing their outputs, and taking appropriate action when disagreement is detected. Finally, selected equivalent functions will be subject to the conventional testing

(1) The apparent duplication of execution cost may be reduced by alternating codes during successive "passes", where this is possible.

and inspection approach, and records kept of the performance and cost of both approaches.

The Time-difference based Loran approach procedure tries to cope with a major objection to the use of Loran-C for non-precision approaches: the use of corrections for signal propagation anomalies.

Due to variations in the propagation characteristics of the terrain between a Loran station and a receiver position, the "electric" grid of hyperbolas of constant time-differences is "distorted" with respect to the "geometric" grid of constant distance-difference hyperbolas. This difference can be of the order of half a microsecond in time difference, or 150 meters in position. On the other hand, it is contended that these differences are repeatable within 0.1 microseconds, or some 15 meters, leading to the suggestion that correction terms be used to achieve 15 meter type performance. This suggestion is viewed with concern by certification authorities because it may lead to blunders (if entered manually) or complex secular changes (similar to magnetic variation, but infinitely more complex). To make matters worse, there is disagreement on the procedures that must be used to convert time differences to latitude and longitude, and differences in the navigated position of different types of Loran receivers have been traced to differences in the mathematical generation of the geometric grid.

The proposed technique is to base the navigation solution for the approach entirely on time-differences, i.e. navigate on the electric, rather than the geometric grid. In this procedure, the "Loran approach" is based on five parameters: two time differences at each end of the runway, and the distance between these points, namely the runway length.(1) The benefits of this technique are twofold: a reduction of the complications (and potential errors) resulting from the use of propagation corrections and various lat-lon conversion schemes, and a reduction of the complexity of the navigation computations required during approach, which can lead to faster display update rates.

(1) Additionally, some approximate information about the location of the airport with respect to the stations may be used to improve the linearity of the approximations involved, particularly at airports situated close to a Loran station; but in any case the navigation solution guides to time-differences, not to a point in lat and lon.

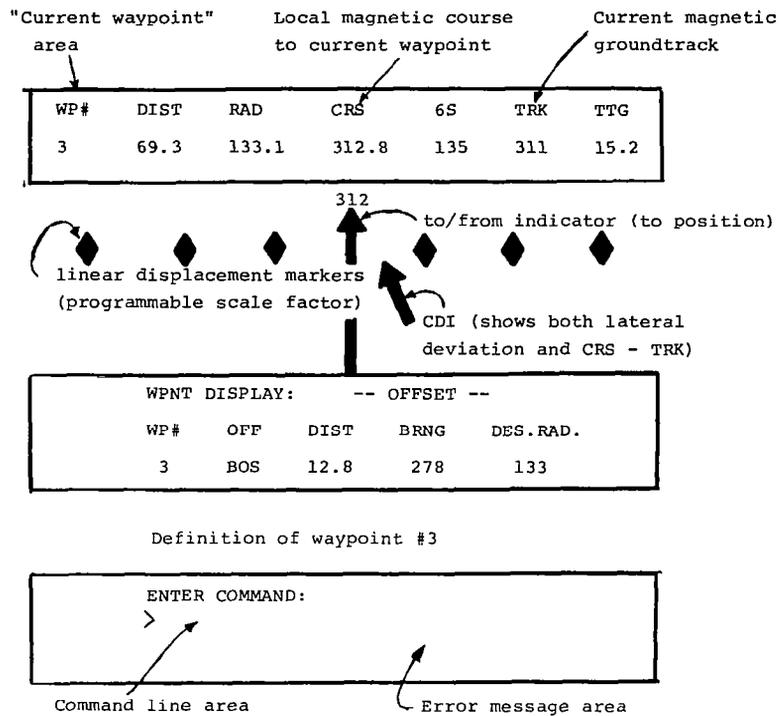


Figure 1. Loran-C navigator commands.

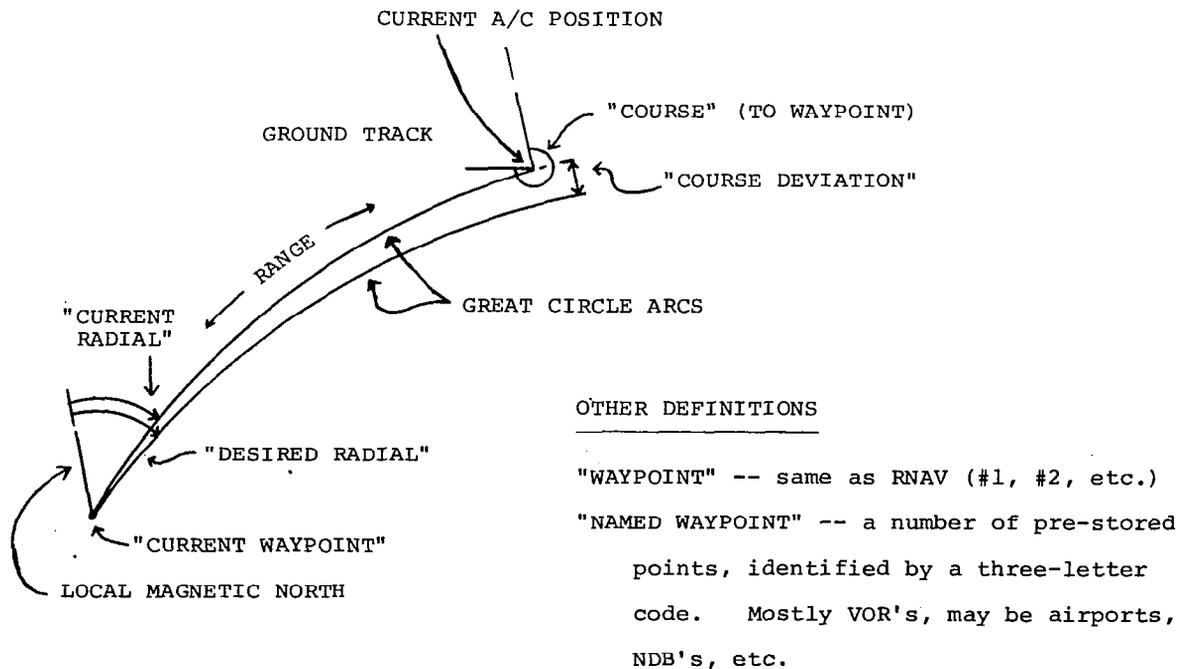


Figure 2. Enroute Loran navigation - geometry and definitions.

```

E -- enter new waypoint in waypoint list

I -- insert new waypoint in waypoint list

D -- delete a waypoint

A -- advance the "current waypoint" to the next
    waypoint in the list

B -- back up the "current waypoint" to the previous
    waypoint in the list

S -- show a waypoint (from the waypoint list) in
    the waypoint display area

T -- set CDI tracking to the "TO" position

F -- set CDI tracking to the "FROM" position

R -- set desired tracking radial to/from a waypoint

```

Figure 3. Summary of Loran-C navigator commands.

PROGRAM MEMORY

ITEM	SOURCE LINES	CODE (BYTES)	
PL1 CODE	706	7177	(10 BYTES/LINE)
ASSEMBLER CODE	365	511	(1.4 BYTES/LINE)
SYSTEM CODE:	-	6522	
TOTAL PROGRAM MEMORY:		14210	

ESTIMATED SAVINGS AND PENALTIES

(PL1 VS. ASSEMBLER)

- MEMORY PENALTY: 4000 BYTES (10000 VS 14000)
- SOURCE CODE SAVINGS: 6000 LINES (1000 VS 7000)

Figure 4. Core and memory usage summary - enroute Loran navigation pilot interface software.

THE P-POD PROJECT: PROGRESS REPORT

James A. Littlefield
MIT, Flight Transportation Laboratory

P-POD PROJECT: PROGRESS REPORT

The programmable pilot oriented display (P-POD) is a multiprocessor based flight information processing and display unit. Most of the work to date has been directed toward optimizing communication protocols between the three Z-80 processors inside P-POD. As described in a previous report, one processor (P0) is dedicated to IO control, data buffering, and formatting; a second processor (P1) is reserved for coordinate transformations and supervision of the other two Z-80's; the third unit (P2) is dedicated solely to display generation.

At the last quarterly meeting of the Tri-University program a description of the interface between the video processor, P2, and the main processor, P1, was given. Subsequent reliability testing led to significant revisions in both hardware and software. Figure 1 illustrates the cycle of data flow between P1 and P2. Should a failure (either hardware or software timing) occur at any point in the data transmission cycle, the process will hang indefinitely, resulting in cessation of display generation and an overflow of the P1/P2 command buffer. While running diagnostic routines to exercise the P1/P2 interface at maximum speed an intermittent failure was observed. A careful check of possible noise sources or race conditions in the hardware diagramed in figure 2 did not reveal the source of this failure. Possible software timing problems were also fully investigated. Due to the sporadic nature of this failure it was not possible to isolate its source; however, all test results point to a portion of the status generation circuit on the video board as the error source.

To eliminate the effects of this type of failure a performance monitor routine is now being used to detect these occasional failures and correct for them. This software correction for hardware failure was deemed prudent for two reasons; detailed debugging of the video board would be very time-consuming with the available documentation; these failures are serious and might be induced by external noise sources. At present,

the real time clock on board P1 is used to trigger execution of a routine which observes the history of interface operation over the previous second. Based on the setting of a flag and contents of a status byte, the data transmission cycle between P1/P2 is either allowed to continue normal operation or is re-initialized and restarted when an error condition is detected.

One of the advantages of a software reliability monitor is that it will correct for any temporary operational failure in the interface (i.e., power line spike, missed interrupt, software timing error, EMI). In addition the assembly coded monitor routine occupies less than 41 bytes. The performance check routine runs every second in the current implementation. Since all commands to the graphics processor, P2, are buffered, no bytes are lost due to momentary hardware failures of the type observed. Command buffer contents are preserved until the transmission cycle is restarted by error detection code. An additional function of the performance monitor is accumulation of a total error count indicating the number of failures detected and corrected since system startup. Presently failure rates of approximately $6/(3 \times 10^5)$ bytes are being observed.

Loran data processing has been the second major area of work during the past quarter. Two 8-bit latches have been connected to the Loran receiver data bus. Whenever new data is latched into these buffers a mode 1 Z-80 interrupt is sent to P0. P0 multiplexes the 16 bits of data onto its own 8 bit IO port by cycling the tri-state enable lines of the octal latches. Once Loran data has entered the P0 memory map it is processed by the control program outlined in figure 3.

The Northstar 6000 receiver is capable of transmitting digital data to four external devices (D0-D3). Data for each of these devices is multiplexed onto the same data bus. IUSER3, the P0 control program, decodes 2 of the four available devices. D1 data consists of TD's for the first and second slaves in the selected chain. D2 data is composed of TD's, SNR's, ECD's, mode numbers, and latitude/longitude for all stations in the chain. D1 data is available once every 2 seconds.

D2 data is available about every 2.7 seconds. IUSER3 will observe both D1, D2 data and transmit either or both to P1 via a DMA operation. IUSER3 can also be configured to select the best data source; if the first and second slaves have high enough SNR's, then D1 data is preferred since it is available more often. SNR's are determined by observing the D2 data stream at all times. Should first or second slave SNR's fall below a programmed threshold value, the D2 data stream will be sent to P1. Whenever data is transferred to P1 memory, the first byte of the transmit buffer contains a tag indicating the contents of that buffer (D1, D2 data).

Use of the additional I0 processor frees the P1 processor from several tasks. The P0 control program formats each data frame and does length checking to ensure that each frame is complete. Thus P1 is assured of having a valid position fix before attempting coordinate conversion.

Objectives for the next quarter are completion of the interface between the P0 control program and the existing PL/1 Loran data processing code which was demonstrated at Ohio University. Successful flight testing of this configuration will be followed by some execution speed tests to more fully document the performance of the interprocessor communications package. Final documentation will complete my thesis work. The interprocessor communications package will provide subsequent users of PPOD with a modular operating environment which will ease adaptation to a wide range of experimental goals.

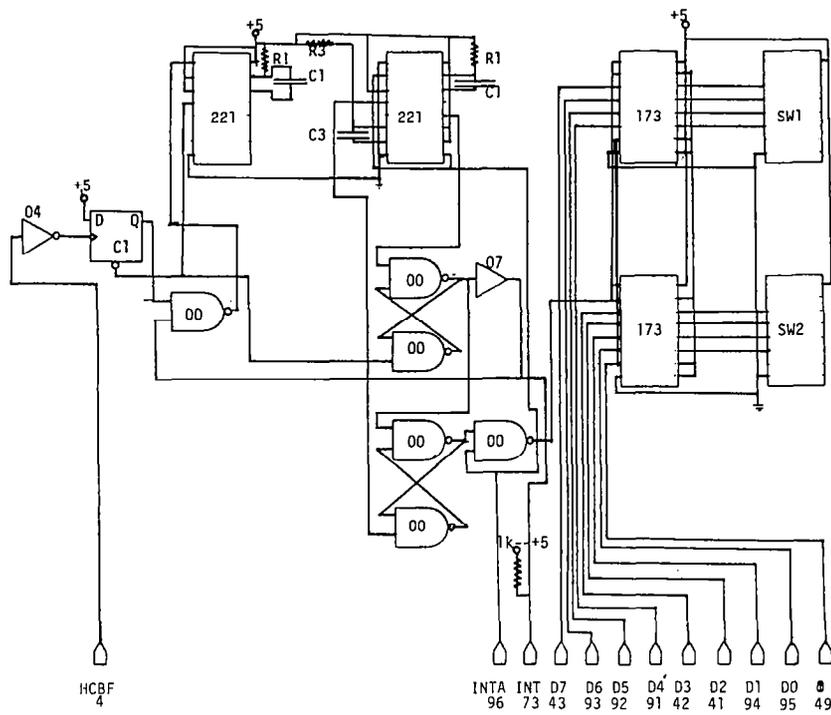


Figure 1. Interrupt jammer rev. 2.

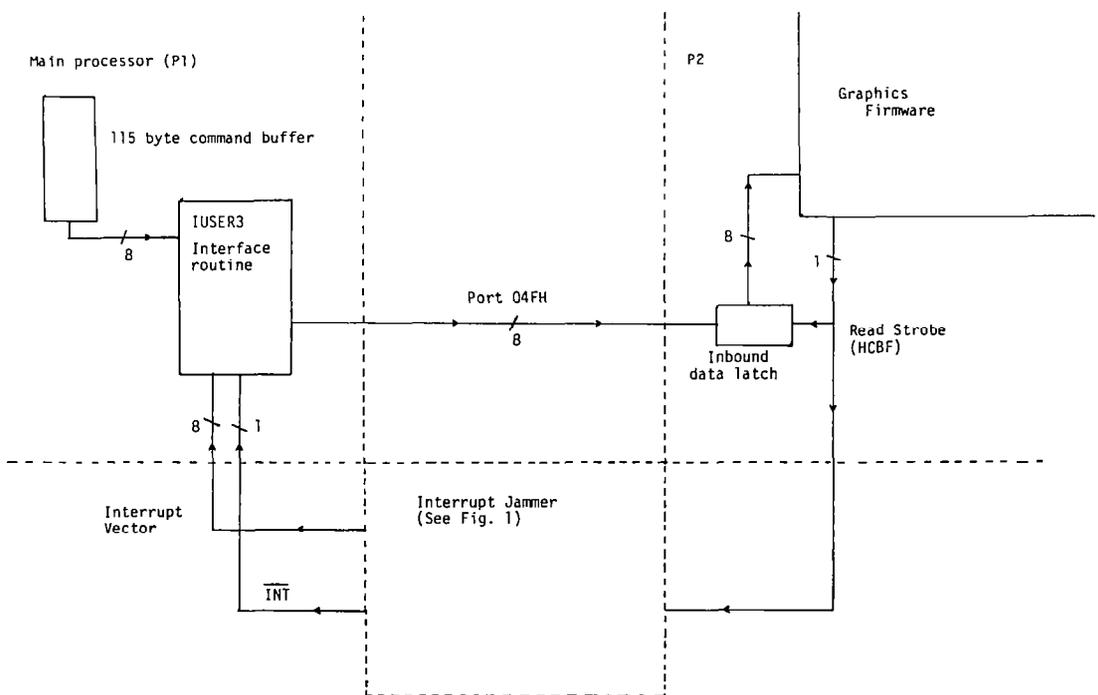


Figure 2. P1/P2 communication data flow.

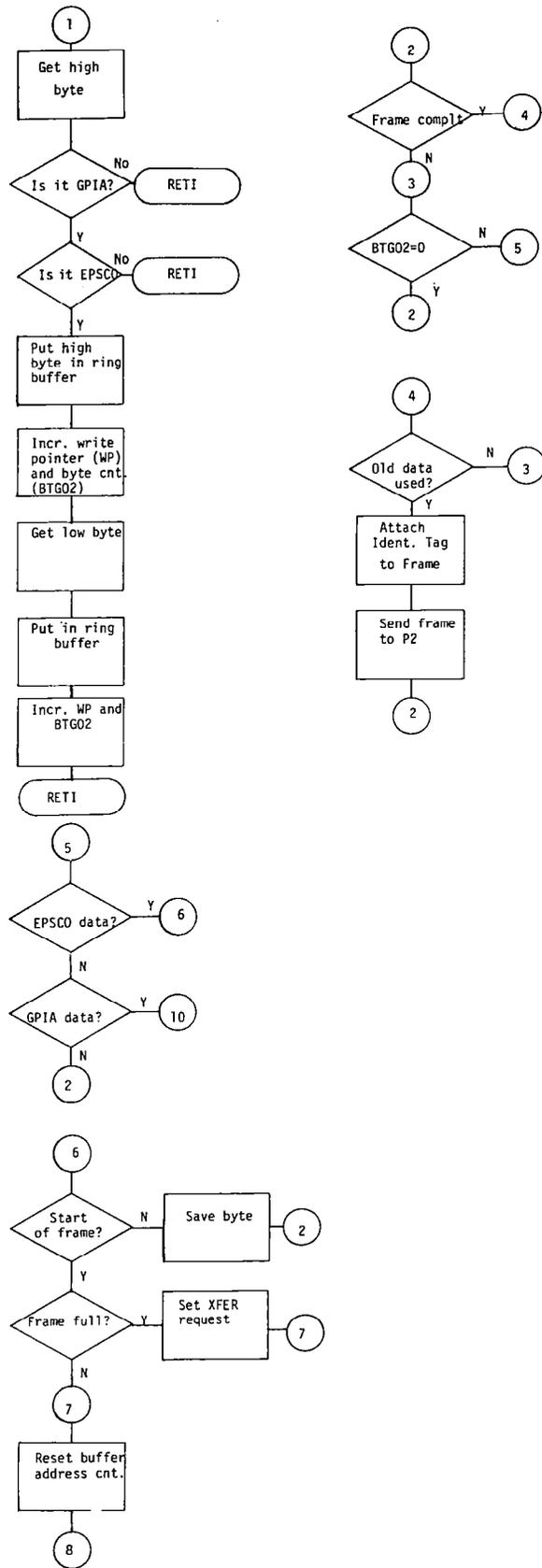


Figure 3. 1USER3 flowchart.

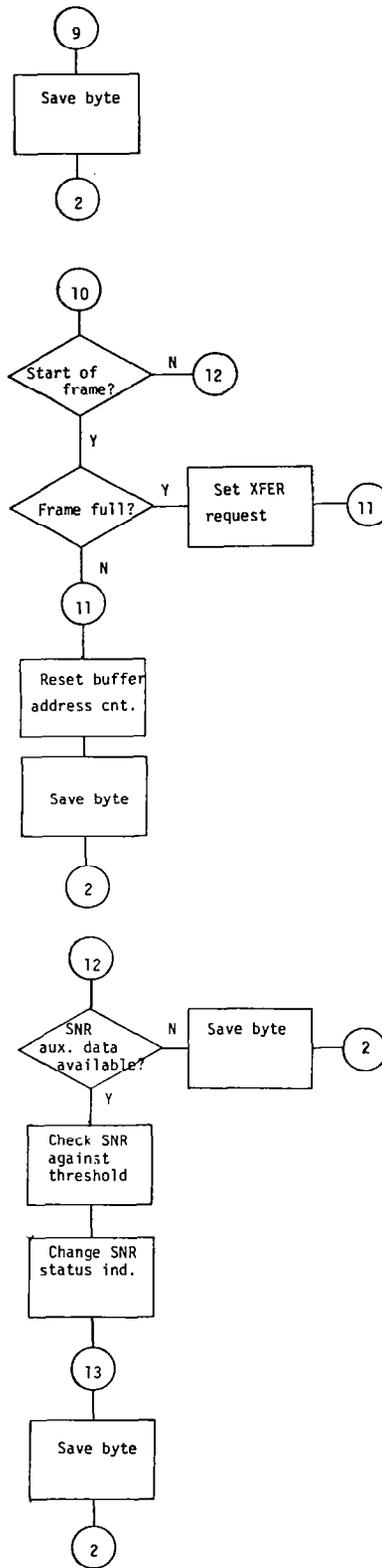


Figure 3. (Concluded).

MICROWAVE ICE PREVENTION

R. John Hansman, Jr.

and

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RESEARCH ON ANTI-ICING BY MICROWAVE HEATING OF SUPERCOOLED WATER DROPLETS

The study of the novel concept of using microwave energy to provide aircraft ice protection, specifically an anti-icing system, and the feasibility of such a system is the aim of this research. In a microwave anti-icing system impinging supercooled water droplets are heated to above freezing by the resonant absorption of microwave energy located upstream of the airfoil. This process is inherently more efficient than existing anti-icing devices due to the saving of the latent heat of fusion (a substantial 334 joules/gm (80 cal/gm)) and the fact that only the droplets are heated, thereby reducing convective losses to the air.

Efficiency improvements of factors of 10 or 20 are, in principle, possible. This would make anti-icing feasible in applications where less desirable de-icing devices are now used. The light weight and low aerodynamic drag of microwave systems are also desirable characteristics.

In studying the microwave anti-ice concept three major issues became obvious:

1. Is there sufficient time to heat the supercooled water droplets? (i.e., will it work?)
2. What efficiencies are realistically possible?
3. What are the applications problems? (i.e., cost, high frequency, interference, runback, etc.)

The work to date has been focused on the first two questions.

The question of droplet heating time has been approached on both a theoretical and experimental basis. The theoretical work has resulted in a model for the heating of a droplet as it approaches an airfoil. The model has undergone several levels of refinement and is manifest in a computer code which calculates droplet trajectories and temperatures. At present, the model includes the following

effects or assumptions:

Rayleigh-Gans absorption

Inviscid airflow around body

Electromagnetic field (can be varied -- normally exponential radial, \cos^2 angular behavior)

Droplet trajectories -- iterative solution of equations of motion from reference 1

Increased heating due to:

droplets slowing before impact

increased absorption from flattening due to pressure gradients

Polarization and near field effects

Evaporative and convective losses

Max. electric field limited by gaseous breakdown

The code is 75% complete and when completed should provide detailed design and efficiency data. Hand calculations of droplet heating including the above effects indicate that there is clearly time to heat the droplets if the microwave frequency is sufficiently high. Pending completion of the code calculations the operating frequency is expected to be between 10 GHz and 30 GHz.

One effect which is considered important but was not included in the above computer simulation due to a lack of a quantitative model is the increase in droplet absorption as it passes through the ice-water phase transition. An increase in absorption is expected at the phase transition due to the nonspherical shapes of freezing and melting droplets.

The theoretical work described above is being supported by an experimental program. The predictions of droplet trajectories and droplet flattening are being compared with wind tunnel investigations of droplet flow around cylindrical and airfoil shapes. Velocity and flattening information are obtained from fast strobe photography and fixed "time of flight" photography in a rain-fog section of the MIT

1 ft by 1 ft tunnel. In addition an experiment is being set up to quantify droplet absorption through the ice-water phase transition. This sensitive measurement is made by observing the change in Q ($Q = \text{power stored}/\text{power dissipated}$) of a resonant cavity which contains melting or freezing water droplets. For more details of the experimental or theoretical work to date, see figures 1 through 17, which were presented at the NASA Joint University Air Transportation Research Conference.

With the completion of the computer simulation of droplet heating and its experimental verification the question of whether there is sufficient heating time will be answered, and we are therefore prepared to begin the next phase of the work. This phase consists of two parallel tasks.

(1) Proof of principal experiment, consisting of the design of a microwave anti-icing system using the above analysis. The system will be mounted on an airfoil section and tested in the wind tunnel. The system can be tested both at room temperature and at icing temperatures (the winter operation of MIT 1 x 1 tunnel is adequate for this purpose). Measurements can be made of microwave power drain and of droplet temperature. The temperature measurement can be made in situ by using advanced fiberoptic thermometry which allows an unperturbing measurement of temperature even in the presence of microwave fields.

(2) Completion of droplet heating work by measuring absorption during the ice-water phase transition described earlier. This work should provide some insight into both the "mixed phase" icing conditions about which there is only limited information and the phenomenon of the "bright band".

REFERENCE

1. Bergrun, Norman R.: A Method for Numerically Calculating the Area and Distribution of Water Impingement on the Leading Edge of an Airfoil in a Cloud. NACA TN 1397, 1947.

	<u>CLOUD DROPLETS (FAR 25)</u>	<u>FREEZING RAIN</u>
T	0 → -20°C	0 → -5°C
LWC	0 → 1 gm/m ³	0 → 3 gm/m ³
D	10 → 40 μm	1 → 5 mm

Generally below 10,000 ft in localized layers and zones

PROBLEM BECAUSE OF:

weight	ice-ingestion
drag	antenna
flutter (anti-ice)	

CURRENT TECHNIQUES

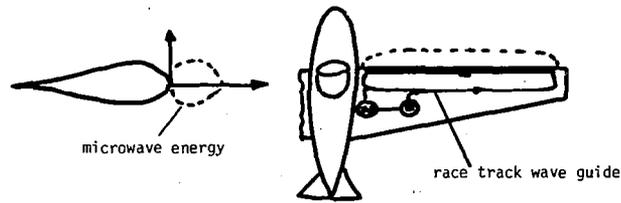
boots	hot air
electrothermal	liquid-glycol or alcohol, TKS

Figure 1. The general parameters of the icing problem and the current techniques used to deal with it.

1. Ice prevention -- use resonant absorption properties of water
 - A. Anti-Ice (Preheat Droplets)
 - B. De-Ice (Melt Ice)

2. The possibility of using radar to remotely detect and avoid icing zones was first proposed by David Atlas in 1954 J. Met. Vol. 11, p. 309, while his concept was based on a ground weather radar, advances in "on board" radar capability along with certain scattering characteristics of droplets at the ice-water phase transition (to be discussed) may make remote detection feasible. Requires vertical scan.

Figure 2. Several concepts of using radiation for ice protection or remote detection. The idea of remotely detecting icing zones by air or ground radar is intriguing and was spawned by meteorological radar observations of a highly-reflecting "bright-band" at the melting layer in precipitation.



This scheme operates in two modes: anti-ice or de-ice

ANTI-ICE

Droplets are preheated to above freezing before impact

Power requirements estimated ($V = 200$ mph, $20 \mu\text{m}$ droplets)

Wing 40 watts/linear foot

Prop or Rotor 25 watts/linear foot (Goodrich "Hot Prop",
200 watts/linear foot)

DE-ICE (Magenheim)

Ice on surface waveguide causes the effective thickness of the dielectric to increase which causes the wave to be more tightly bound. The high fields which result cause heating at the ice-dielectric interface, thus unbinding the ice from the surface.

Figure 3. One possible scheme for using radiation for ice prevention, primarily anti-icing. First-order conceptual scheme employing surface waveguides.

- (1) Only water heated -- low convective losses
- (2) Saves latent heat

$$L_{iW} = 80 \frac{\text{cal}}{\text{gm}} \quad L_{wV} = 600 \frac{\text{cal}}{\text{gm}}$$
- (3) Only draws power when liquid water present (i.e., serves as its own detector)
- (4) Aerodynamically clean
- (5) Low maintenance
- (6) High power microwave technology on a strong growth trend

Figure 4. Several potential advantages of a microwave anti-icing system.

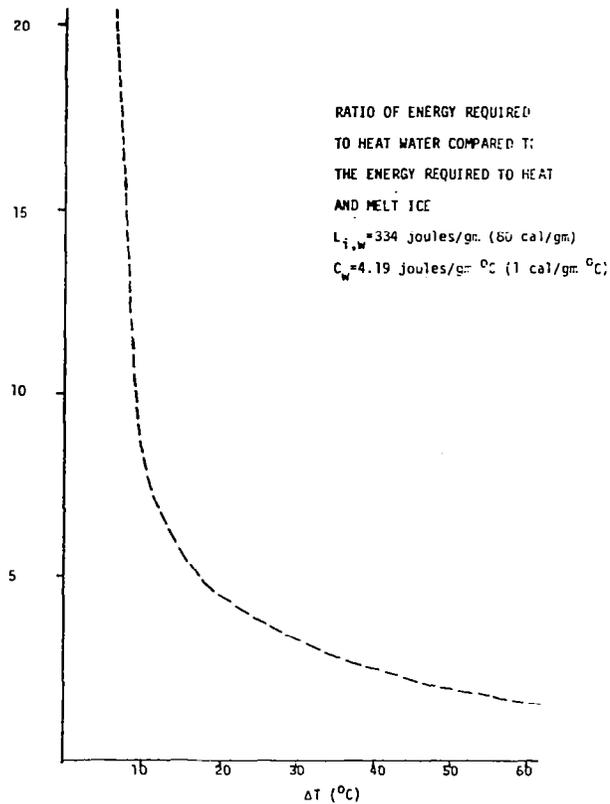
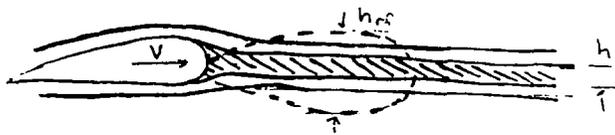


Figure 5. Efficiency improvement gained by avoiding the loss of the latent heat of fusion at the ice-water phase transition (80 ml/gm). Note that a similar but greater effect occurs with the latent heat of evaporation (600 cal/gm).

1. Is there sufficient time to heat the droplets? i.e., what are the absorption properties of the impinging droplets?
2. How well can the RF energy be focussed determines effectively



efficiency goes as h_i/h_{rf} implies shorter wavelength desirable
 $h_i \sim 1 \text{ cm}$

3. Runback refreeze problems
4. Applications problems (i.e., cost, HFI etc)

While all the above are important, the most germane is #1.

Figure 6. Major questions which must be addressed in order to determine the feasibility and operating frequency of a microwave anti-ice system.

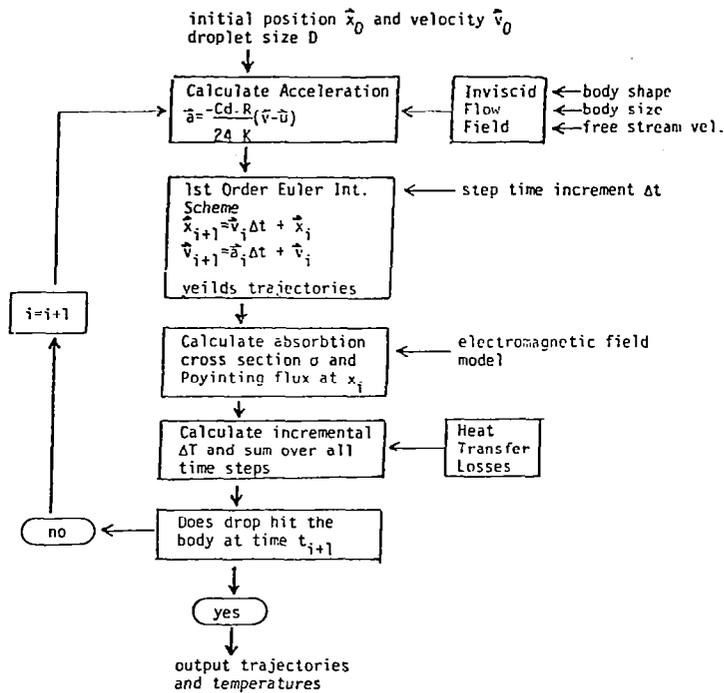


Figure 7. Flow chart for a computer simulation of droplet trajectories and heating. This code has been written to help address the questions of droplet heating time and efficiency. The absorption cross section includes Rayleigh or Mie absorption, with pressure-induced shape effects, polarization, and phase effects included. Equation of motion is from reference 1.

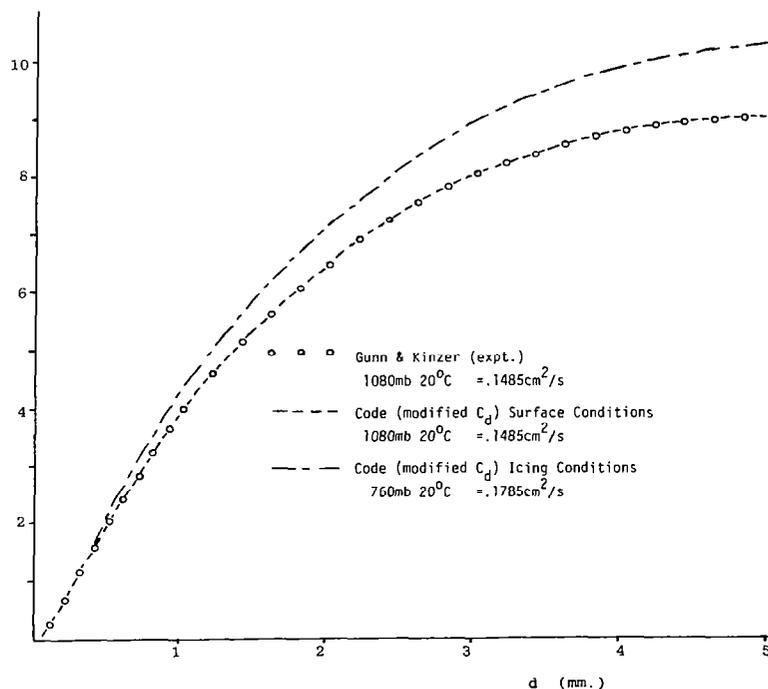


Figure 8. Computer-calculated trajectories are checked by computing the terminal fall velocity of drops (m/sec) versus droplet diameter (mm). With the drag coefficients modified to include droplet flattening the code is in good agreement with established experimental data.

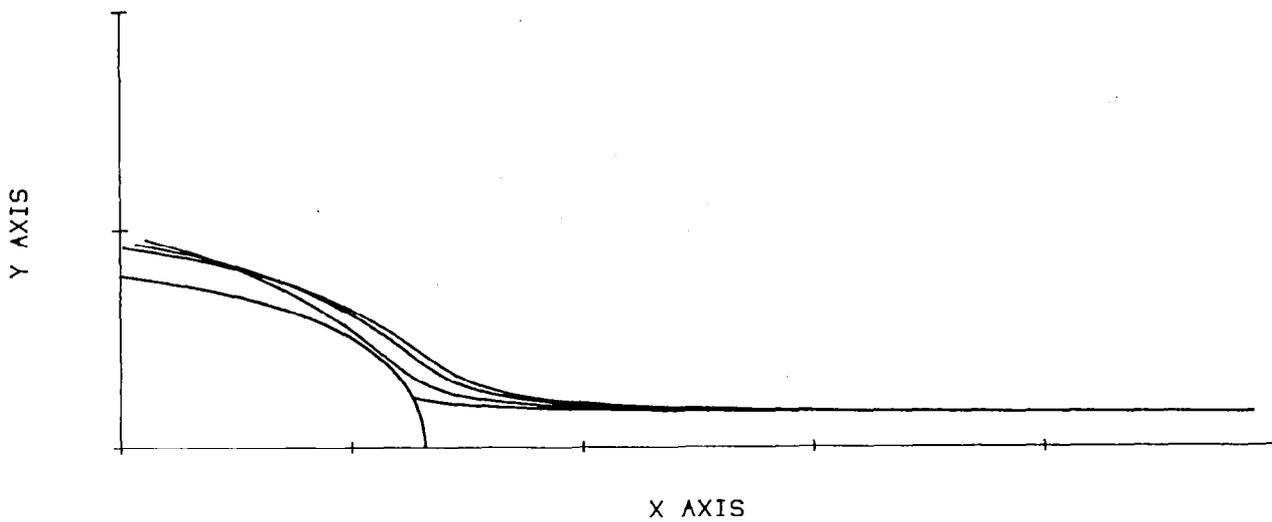


Figure 9. Droplet trajectories near half body. Droplets of four different sizes, 5, 10, 20, and 40 μm , approach a "half-body" airfoil. The smaller droplets are accelerated around the body while the larger droplets impact. The effect of the increasing catch efficiency with droplet size is discussed in figures 10 and 11.

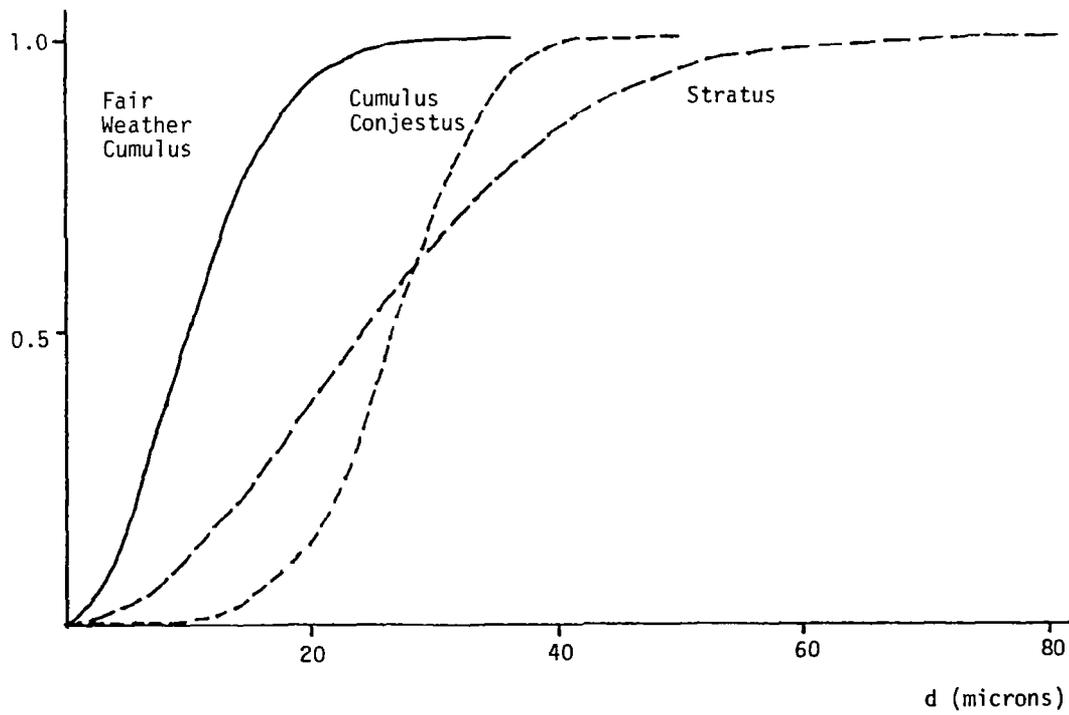


Figure 10. Fraction of liquid water with diameter smaller than d , showing typical droplet size distributions in several different types of clouds.

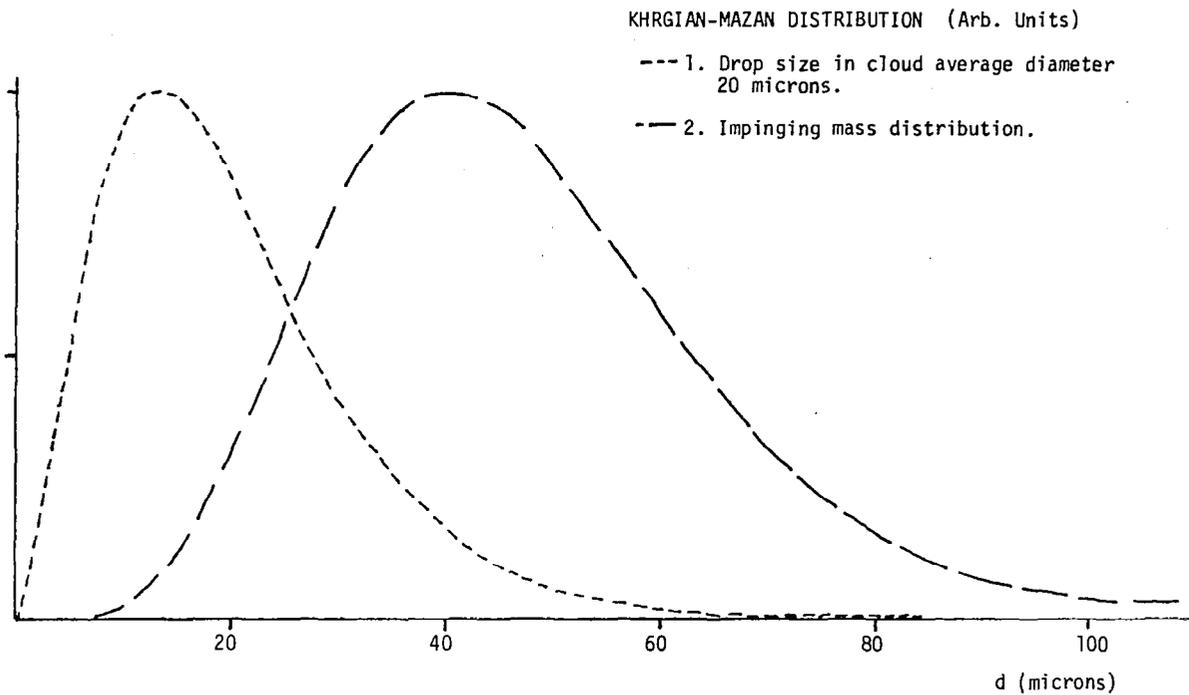


Figure 11. Illustration of the effect of the larger droplets being caught more efficiently by the airfoil. The larger droplets contribute appreciably more to the icing mass than the more prevalent smaller droplets.

Current anti-ice systems evaporate all water

$$L_{WV} = 600 \text{ cal/gm} \quad C_W = 1 \text{ cal/gm K}$$

Preliminary heat transfer calculations over wet wing show factor of 10 to 20 improvement over evaporative systems

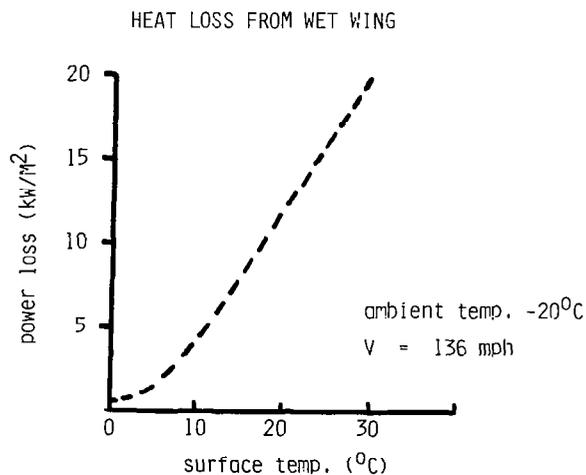


Figure 12. Some preliminary calculations of heat loss during runback. It is clear that the coolest feasible surface temperature is the most desirable for an electrical system, as opposed to the 20° to 30°C temperatures used in hot air systems.

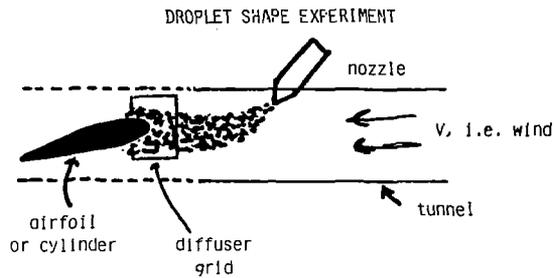
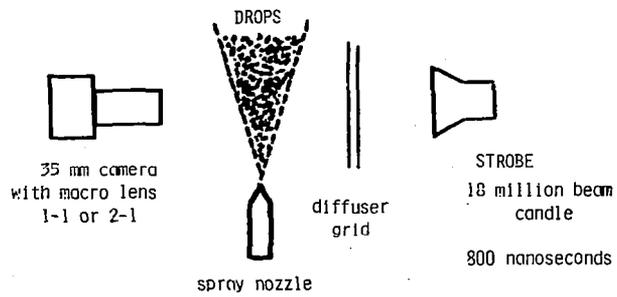


Figure 13. Photographic setup used to attempt to validate the computer simulation of droplet flattening and trajectories.

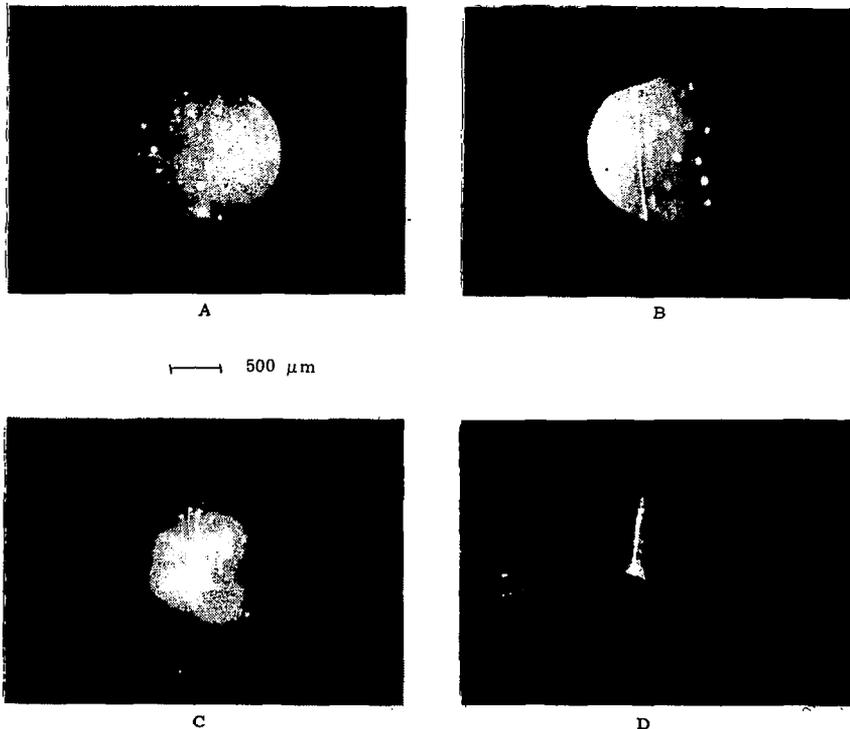


Figure 14. Photographs taken on the stagnation streamline of a 4.4" diameter cylinder with a free-stream velocity of 60 mph.

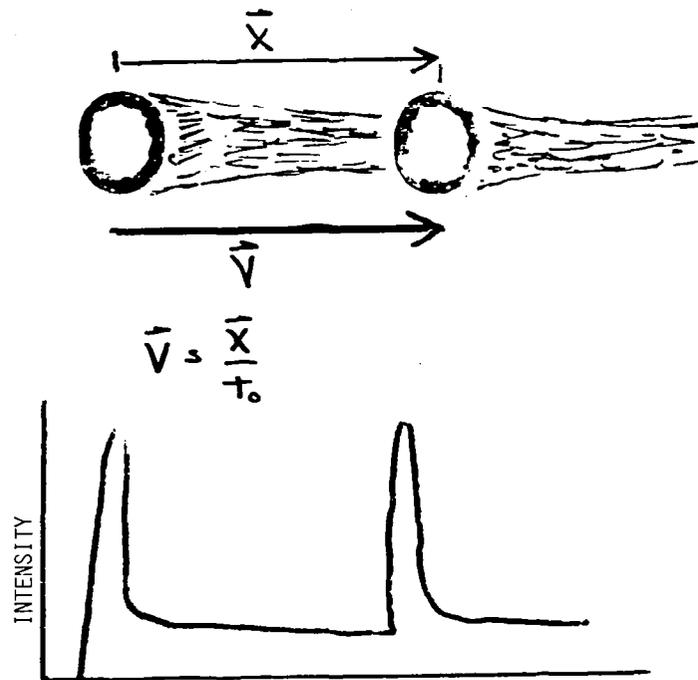


Figure 15. Droplet velocity measurement by double strobe photography.

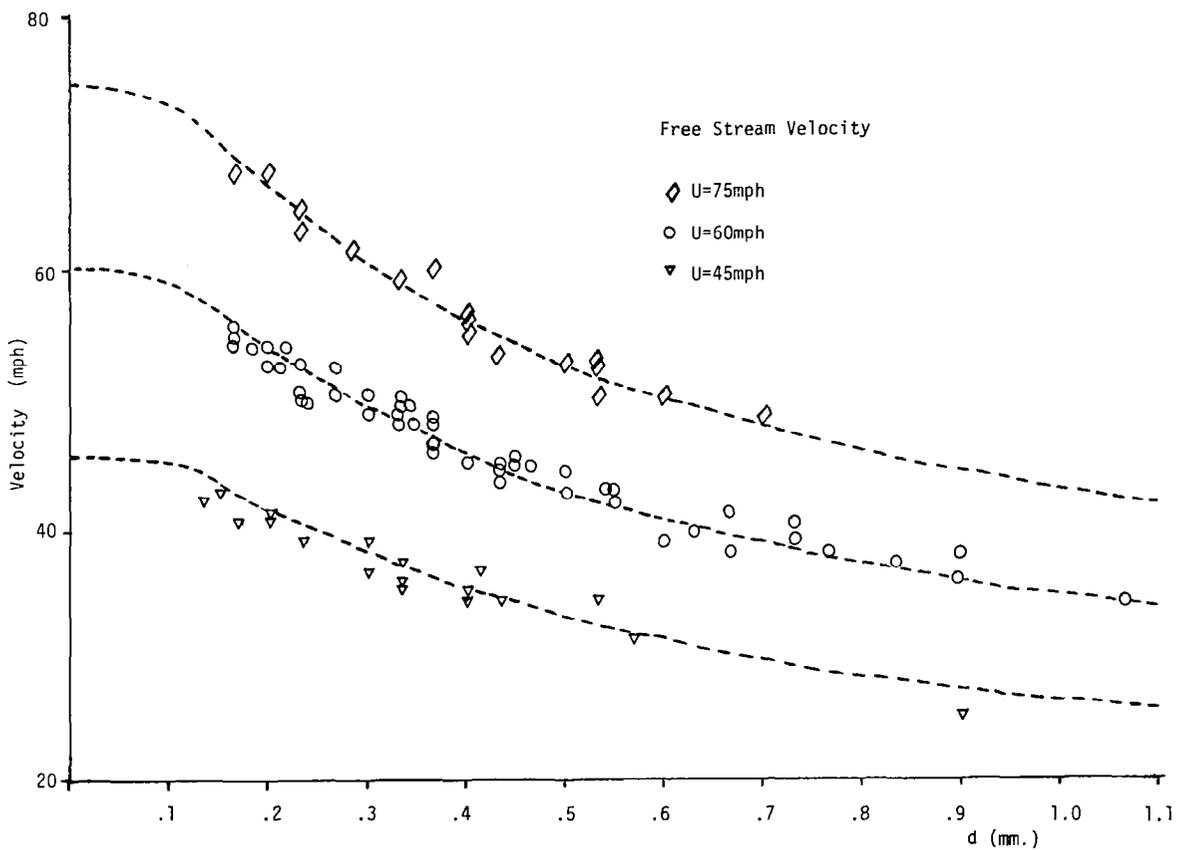


Figure 16. Plot of velocity along tunnel axis (1.25 m downstream of injection site) versus droplet diameter for droplets injected into an unobstructed tunnel. These velocity measurements were made by the technique described previously and are in good agreement with the computer simulation values (dashed lines).

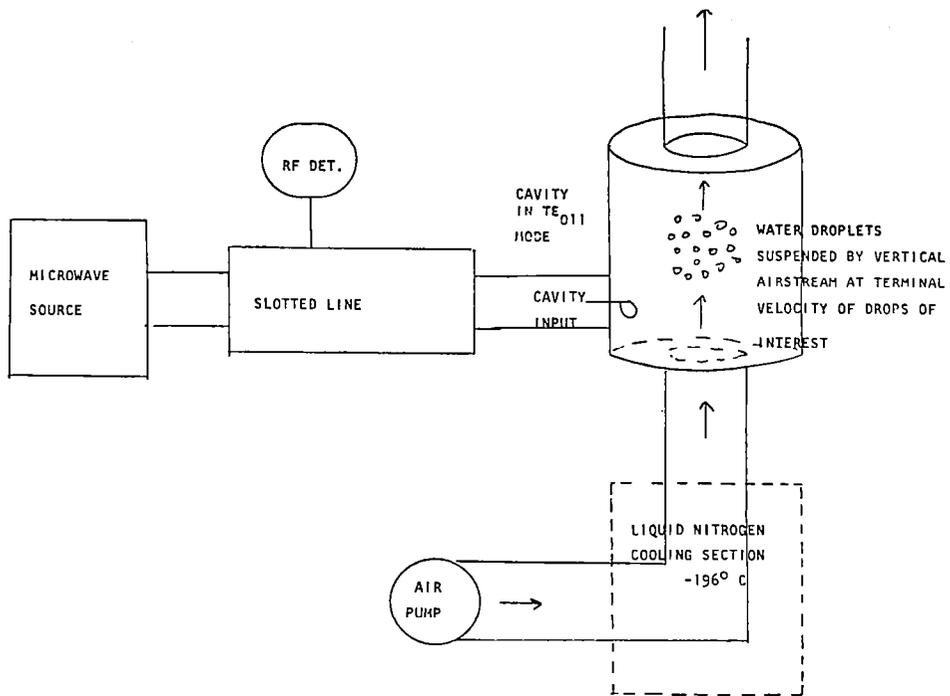


Figure 17. Schematic of phase-change absorption experiment being done to quantify absorption of droplets as they pass through ice-water phase transition.

Ohio University

INVESTIGATION OF AIR TRANSPORTATION TECHNOLOGY

AT OHIO UNIVERSITY, 1981

Professor Richard H. McFarland
Avionics Engineering Center
Department of Electrical Engineering
Ohio University
Athens, Ohio 45701

INTRODUCTORY REMARKS

Loran-C has had much of its development motivated by military and marine applications. The increased availability of Loran signals in the United States has encouraged consideration of Loran for airborne applications and has motivated a somewhat similar evaluation and approach as was performed by Ohio University several years ago in this NASA-supported joint university program then using Omega navigation.

The low-frequency band because of its relatively high noise contamination, requires high-quality signal processing to obtain effective signal-to-noise ratios which permit good reliability in position determination consistent with airborne applications. To this end Ohio University has investigated techniques for deriving air-navigation quality information from Loran-C. A part of this objective has been to produce the navigation data in as efficient and cost-effective a manner as possible. Specifically, the volume, weight and power requirements of the equipment are to be compatible with light airplane flown in the general aviation environment.

The Lilley-McCall paper describes the effort which led to a prototype Loran-C receiver which was designed, built and flight tested as a part of this year's work effort. Two undergraduate students, two graduate students and two staff supervisors worked on this project for over a year. The final results have been to produce a receiver which, for demonstrations, operates with a master-dependent, single chain tracking three stations.

The Burhans paper which follows reveals the development of the RF circuitry. During the evolution of this receiver prototype, students in particular have also obtained rich experiences in microprocessor applications, software development, fabrication techniques and final proofing of concepts by measurements of navigation performance in flight on board a Piper Cherokee and a Douglas DC-3.

The use of a navigation receiver during flight leads to consideration of several ancillary aspects of the navigation equipment itself. One consideration is the development of a more intuitively satisfying and useful reference coordinate frame. The hyperbolic geometries inherent in the Loran time-difference system are not easily used by pilots; consequently, a

coordinate conversion is highly desirable. One approach to a coordinate conversion uses an on-board microprocessor for producing the convenient and common polar coordinate geometries available with contemporary VORTAC navigation.

Finally, and with work in progress, the concern is with the human interface. Display of the navigation information in a manner which is consistent with the general aviation cockpit environment and in a form which is convenient and conducive for interpretation by the pilot is the goal. Completion of the display work described by Novacki will mean that the project has been involved with a totality of aspects of the Loran-C airborne equipment ranging from conceptualizing and design to flight testing. Further movement along this line will take place with colleagues at MIT obtaining data on performance and pilot usage of the equipment.

Following also are a bibliography of reports and presentations of reports completed during 1981 on the tasks integral to the Loran airborne receiver developed at Ohio University.

The reports referred to as OU NASA TM-XX in the papers and in the annotated bibliography are the work of Ohio University and should not be confused with the NASA TM series of reports, which are represented by five-digit numbers (NASA TM-XXXXX). Research done at Ohio University under the Joint University Program is supported by NASA and reported in the OU NASA TM-XX series. These reports may be obtained from the University directly.

FIRST TECHNICAL AREA - OMEGA NAVIGATION

DEVELOP TECHNOLOGY TO MAKE OMEGA SUITABLE FOR GENERAL AVIATION

- RF CIRCUIT DESIGN
- SIGNAL PROCESSING
- RECEIVER DESIGN
- FLIGHT EVALUATION

IDENTIFY FUNDAMENTAL PROBLEMS AFFECTING GENERAL AVIATION

- NOISE FACTORS
- GEOMETRIES
- PROPAGATION FACTORS
- ACCURACY REQUIREMENTS

SECOND TECHNICAL AREA - LORAN-C

DEVELOP TECHNOLOGY MAKING LORAN-C APPLICABLE TO GENERAL AVIATION

- RF CIRCUITS
- AGC
- ENVELOPE DETECTION
- PROTOTYPE RECEIVER

INVESTIGATIONS OF NOISE EFFECTS

PHASE-LOCK TRACKING LOOPS

APPLICATIONS OF MICROPROCESSOR TECHNIQUES TO LORAN-C

COORDINATE CONVERSIONS

DISPLAY INTERFACE

BENEFITS

TECHNOLOGY PRODUCT - 82 TECHNICAL MEMORANDUMS

STUDENT PRODUCT - OVER 31 GRADUATES
(BSEE, MS AND PHD LEVELS)

STUDENT IMPROVEMENT IN THE LAB AND CLASSROOM

INDUSTRY BENEFITS - TECHNICAL INFORMATION PROVIDED TO MORE THAN
100 CONTACTS. EXAMPLES ITT, LITTON, TELEDYNE,
MAGNAVOX, ROCKWELL

ANNOTATED BIBLIOGRAPHY

OU NASA TM Number

- 1 SIMULTANEOUS PAIR OMEGA RECEIVER
Ralph W. Burhans, August 4, 1972.

A new concept of OMEGA receiver operation is presented. The simultaneous comparison of 13.6 and 10.2 KHz in a single time slot results in 3.4 KHz, 10.2 KHz, and phantom 40.8 KHz difference pair lanes. Direct lane count without intermediate storage or sequential feedback loops is possible. Small boat receivers using low cost recorders such as a Rustrak might be possible at \$300 market prices. Completely digital readout devices for general aviation use could become \$500 instruments. Even with restricted lane pair use this could provide low cost navigation aids for over half of the U.S.A. and all of the coastal areas including most of the Great Lakes.

- 2 SIMPLE BAND PASS FILTERS
Ralph W. Burhans, December 28, 1972.

A single power source operational amplifier provides tunable-high Q band pass resonators of possible utility for OMEGA VLF receiver input processors and other audio frequency applications.

- 3 LOW BIT SINE WAVE APPROXIMATIONS FOR AUDIO SIGNAL SOURCES
Ralph W. Burhans, January 1973.

Special purpose sine wave sources are easily obtained using digital counting-decoder-filter methods with second harmonic distortion less than 1%. Good frequency stability and reasonable variety in choice of output frequency result when the input clock signal is derived from a crystal oscillator through programmable divider chains. The resulting sine wave output would be suitable for applications such as the 90 and 150 Hz modulation frequencies of ILS transmitters, as well as other limited range audio frequency use.

- 4 SIMPLIFIED OMEGA RECEIVERS
Ralph W. Burhans, March 1974.

Circuit details are presented for a low cost OMEGA receiver being developed for general aviation use. Some novel processing methods, not used in commercial systems, have been demonstrated in experimental bench processors. An airborne model is being designed.

- 5 BINARY PHASE LOCK LOOPS FOR SIMPLIFIED OMEGA RECEIVERS
Ralph W. Burhans, March 1974.

A sample binary phase lock loop is proposed for periodically correcting OMEGA receiver internal clocks. The circuit is particularly simple to implement and provides a means of generating long range 3.4 KHz difference frequency lanes from simultaneous pair measurements.

- 6 PHASE LOCK LOOP SYNTHESIZER FOR OMEGA REFERENCE FREQUENCIES
Kent A. Chamberlin, April 1974.

An OMEGA reference frequency of 4080 KHz is provided by a single loop VCXO circuit driven from an atomic clock or stable crystal standard. The circuit is used to provide OMEGA frequencies for direct ranging, differential correction monitoring, or as a laboratory source for calibrating OMEGA receivers.

- 7 SIMULTANEOUS MASTER-SLAVE OMEGA PAIRS
Ralph W. Burhans, April 1974.

Master-Slave sequence ordering of the OMEGA system is suggested as a method of improving the pair geometry for low cost receiver user benefit. The sequence change will not affect present sophisticated processor users other than to require new labels for some pair combinations, but may require worldwide transmitter operators to slightly alter their long range synchronizing techniques.

- 8 SELECTED BIBLIOGRAPHY OF OMEGA, VLF AND LF TECHNIQUES APPLIED TO AIRCRAFT NAVIGATION SYSTEMS
NASA Project Staff, August 1974.

A bibliography of references collected during the first three years of the NASA Tri-University Program in Air Transportation Systems.

- 9 LOW-COST OMEGA NAVIGATION RECEIVER
Robert W. Lilley, October 1974.

The status of Ohio University's efforts towards specifying a low-cost Omega receiver is reviewed at the onset of the fourth-year program under the NASA Tri-University Program in Air Transportation Systems.

- 10 BINARY PROCESSING CONCEPTS FOR OMEGA RECEIVERS
Robert W. Lilley, November 1974.

Preprint of paper presented at the Second Omega Symposium, sponsored by the Institute of Navigation, Washington, D.C., November 7, 1974.

- 11 THE MEMORY-AIDED DIGITAL PHASE-LOCKED LOOP
Kent A. Chamberlin, November 1974.

Preprint of paper presented at the Second Omega Symposium, sponsored by the Institute of Navigation, Washington, D.C., November 7, 1974.

- 12 OMEGA FLIGHT-TEST DATA REDUCTION SEQUENCE
Robert W. Lilley, November 1974.

A series of FORTRAN computer programs for preparation and summary of flight-test data obtained from the Ohio University Omega Receiver.

- 13 FLIGHT EVALUATION: OHIO UNIVERSITY OMEGA RECEIVER BASE
Kent A. Chamberlin, R. W. Lilley, and Richard J. Salter,
November 1974.

A description is given of the data-collection flight, round-trip from Athens, Ohio to Langley Field, Virginia, during which Omega data was collected on machine-readable media for use in the Tri-University Program in Air Transportation.

- 14 COMPUTER PROGRAM CORDET
R. A. Palkovic, November 1974.

A simulation tool is described for use in the design and analysis of digital phase-locked loops, with specific application to the DPLL in the Ohio University Omega receiver base.

- 15 A SIMULATION ANALYSIS OF PHASE PROCESSING CIRCUITRY IN THE OHIO UNIVERSITY OMEGA RECEIVER PROTOTYPE (Master's Thesis)
R. A. Palkovic, June 1975 (CR-132707).

A first-order digital phase-lock loop is modeled on the computer. Loop response to signal phase in noise is evaluated. Optimum integration time is determined. Phase jitter in a frequency synthesizer used as the local oscillator is quantified, and design is optimized. Design rules for use of synchronous rate multipliers are presented. Overall system response is discussed.

- 16 GANGED SERIES POTENTIOMETER MIXER NETWORKS
Ralph W. Burhans, December 1974.

A ganged potentiometer with a single linear section and two opposite log tapered sections is rediscovered for providing a simple series resistor control element for mixing of audio frequency signals. An application is for bench evaluation of detector signal-to-noise ratios with Omega receivers.

- 17 COMMON ANTENNA PREAMPLIFIER-ISOLATOR FOR VLF-LF RECEIVERS
Ralph W. Burhans, July 1975.

An improved high impedance preamplifier circuit provides outputs to drive an Omega-VLF receiver and an ADF-LF receiver from a common antenna such as the ADF sense antenna on general aviation aircraft. The preamplifier has been evaluated with fixed ground station receivers and is anticipated for use in the second generation prototype Ohio University Omega receiver design.

- 18 LOW COST, HIGH-PERFORMANCE, VLF RECEIVER FRONT-END
Ralph W. Burhans, September 1975.

A VLF receiver front-end has been designed using standard linear integrated circuits. The basic methods have been evaluated extensively on the Omega 10.2 KHz channel but are readily adaptable to any other VLF frequency in the 10.2 KHz to 20 KHz region. Applications for the modules exist in position location, time-frequency measurements, and signal propagation. The set provides control gates, zero crossing signals, and analog outputs to interface with any type of digital logic, microprocessor, or analog signal processor.

- 19 DIGITAL CORRELATION DETECTOR FOR LOW-COST OMEGA NAVIGATION
Kent A. Chamberlin, February 1976 (CR-144956) (Master's Thesis)

This report describes the background information on the research that led to the development of the memory-aided phase-locked loop (MAPLL) which is an all-digital correlation device that is capable of determining the phase of extremely noisy fixed-frequency signals. This design is of special interest for Omega or other phase sensitive VLF navigation purposes since it is relatively inexpensive, maintenance-free, and can operate in a time-multiplexed fashion.

- 20 THE MINI-O, A DIGITAL SUPERHET, OR A TRULY LOW-COST OMEGA
NAVIGATION RECEIVER
Ralph W. Burhans, November 1975. (CR-144923)

A quartz tuning fork filter circuit and some unique CMOS clock logic methods provide a very simple OMEGA-VLF receiver with true hyperbolic station pair phase difference outputs. An experimental system has been implemented on a single battery-operated circuit board requiring only an external antenna preamplifier and LOP output recorder. A bench evaluation and preliminary navigation tests indicate the technique is viable and can provide very low-cost OMEGA measurement systems. The method is promising for marine use with small boats in the present form, but might be implemented in conjunction with digital microprocessors for airborne navigation aids.

- 21 FLIGHT TEST OF 4-HZ AND 30-HZ OMEGA RECEIVER FRONT-END
Lee Wright, February 1976.

A test flight in DC-3 aircraft was conducted to evaluate the performance of a 4-Hz ultra-narrowband, Omega receiver front-end compared to a more conventional 30-Hz bandwidth receiver. Results indicate that the 4-Hz front-end has superior signal-to-noise performance. Other interesting results obtained during the test flight were recordings of the sunset noise effects on amplitude, and the attenuation of signal levels when flying through clouds.

- 22 POSSIBLE METHODS FOR USSR-VLF NAVIGATION RECEIVERS
Ralph W. Burhans, March 1976.

A brief study of the USSR-VLF navigation system indicates that very low-cost digital techniques might be applied to receiver systems. The transmitted signal format is of interest for application to other VLF systems in the future. Some possible circuits for simplified receiver processors are presented.

- 23 A PROPOSED MICROCOMPUTER IMPLEMENTATION OF AN OMEGA NAVIGATION PROCESSOR
John D. Abel, March 1976.

Documentation of current status of research pertaining to a microprocessor-based Omega navigation processor to be used in conjunction with the Ohio University Avionics Engineering Center Omega sensor processor is presented.

- 24 IMPROVEMENTS FOR OMEGA RF PREAMPLIFIERS
Lee Wright, April 1976

An Omega preamplifier with no phase shift over the ADF band but with bandpass filtering and gain at the Omega-VLF band has been designed, built, and tested. This is expected to be useful principally in planned work at MIT and Princeton involving the use of the Ohio University Omega Sensor Processor Receiver.

- 25 NARROW BAND BINARY PHASE LOCKED LOOPS
Ralph W. Burhans, April 1976.

Very high Q digital filtering circuits for audio frequencies in the range of 1 Hz to 15 KHz are implemented in simple CMOS hardware using a binary local reference clock frequency. The circuits have application to VLF navigation receivers and other narrow band audio range tracking problems.

- 26 SIMULATION ANALYSIS OF A MICROCOMPUTER-BASED LOW-COST OMEGA NAVIGATION SYSTEM
Robert W. Lilley and Richard J. Salter, Jr., May 1976.

Preprint of paper presented at the Bicentennial National Symposium of the Institute of Navigation, Warminster, Pennsylvania, April 28, 1976.

- 27 AUTOMATIC NOISE LIMITER-BLANKER
Ralph. W. Burhans, May 1976.

Modifications of an audio noise limiter circuit, used in WW II era radio communications receivers, provides a noise limiter-blanker for narrow bandwidth low-level audio signals. The method has been evaluated for noise blanking with OMEGA-VLF navigation receivers but is adaptable to more general audio frequency processing systems.

- 28 SMALL AIRCRAFT FLIGHT EVALUATION OF RUSTRAK CHART RECORDER
Richard J. Salter, Jr. and Robert W. Lilley, May 1976.

In support of the NASA Omega Prototype Receiver project, three short flight evaluations of the RUSTRAK chart recorder were flown.

- 29 DIGITAL TIME SLOT DISPLAY FOR OMEGA RECEIVER
Ralph E. Smith, July 1976.

Variations of circuits to display the Omega sequence letters A through H have been designed, breadboarded, and tested. One of these is suggested as an alternative station display method for the Ohio University Omega sensor processor systems.

- 30 LOW-COST MECHANICAL FILTERS FOR OMEGA RECEIVERS
R. W. Burhans, June 1976.

A set of mechanical filter assemblies has been obtained for possible use in the RF front-end of an OMEGA navigation receiver. The resonators provide very narrow bandwidth performance with good skirt selectivity in a simple two-stage circuit. It is recommended that these filters be used in a complete receiver system for long-term evaluation on reception of low-level OMEGA signals.

- 31 A MEMORY-MAPPED OUTPUT INTERFACE: OMEGA NAVIGATION OUTPUT
DATA FROM THE JOLT (TM) MICROCOMPUTER
R. W. Lilley, August 1976.

A hardware interface which allows both digital and analog data output from the JOLT microcomputer is described in context with the Ohio University software-based Omega Navigation Receiver.

- 32 A MICROPROCESSOR INTERFACE FOR THE OHIO UNIVERSITY PROTOTYPE
OMEGA NAVIGATION RECEIVER
R. W. Lilley, August 1976.

A hardware interface is described which allows a microcomputer to obtain data and interrupt signals from the Ohio University Omega Receiver Prototype.

- 33 TEST PROGRAM FOR 4-K MEMORY CARD, JOLT MICROPROCESSOR
R. W. Lilley, August 1976.

A memory test program is described for use with the JOLT micro-computer memory board used in development of the Ohio University Omega navigation receiver.

- 34 A MICROCOMPUTER-BASED LOW-COST OMEGA NAVIGATION SYSTEM
R. W. Lilley and R. J. Salter, Jr., August 1976.

Preprint of paper presented at the First Annual Meeting, International Omega Association, Arlington, Virginia, July 27-29, 1976

- 35 MINI-O, SIMPLE OMEGA RECEIVER HARDWARE FOR USER EDUCATION
R. W. Burhans, August 1976.

Preprint of paper presented at the First Annual Meeting,
International Omega Association, Arlington, Virginia,
July 27-29, 1976.

- 36 OPERATING INSTRUCTIONS: KENNEDY TEST FIXTURE
Donald P. Seyler, September 1976.

A unit for testing the integrity of data and control circuits
of the Kennedy 1600/360 Incremental Tape Recorders is
described.

- 37 OPERATING INSTRUCTIONS: MEMODYNE/KENNEDY INTERFACE UNIT
Donald P. Seyler, January 1977.

A unit for transcribing incremental data from magnetic
cassette tapes to magnetic reel-to-reel tapes is described.
This includes integral testing for validity of data.

- 38 KIM-1 INTERFACE ADAPTER TO 3-WIRE TELETYPE SYSTEMS
R. W. Burhans, August 1976.

This brief technical note has been submitted to the KIM-1
microcomputer group publication, KIM User Notes. It is of
interest to others who have 3-wire ASR-33 teletype systems in
using microcomputer hardware with the Ohio University
Prototype Omega Sensor Receivers.

- 39 OMEGA DISTRIBUTION AMPLIFIER WITH FOUR CHANNEL INDEPENDENT
LEVEL CONTROL
Donald P. Seyler, September 1976.

A portable unit for distributing a single small signal source
to a maximum of four loads, with independent source level
control for each load, is described.

- 40 MEASURING CLOCK OFFSETS FOR MINI-O WITH KIM-1
R. W. Burhans, September 1976.

The previous MINI-O Omega receiver system required adjustment
of the local clock to a low offset for proper operation.
Single station tracking loop software provides an easy way of
determining the offset prior to experimental navigation tests.
A second order software tracking loop is suggested to elimi-
nate the local clock error problem.

- 41-Mod 1 IMPROVED ANALOG OUTPUT CIRCUITS FOR OHIO UNIVERSITY PROTOTYPE
OMEGA NAVIGATION RECEIVERS
Lee Wright, October 1976.

A minor hardware change is described which provides a more
accurate analog output from the Ohio University Omega Prototype
Receivers.

- 42 DIURNAL MEASUREMENTS WITH PROTOTYPE CMOS OMEGA RECEIVERS
R. W. Burhans, November 1976.

The Ohio University Prototype CMOS Omega Sensor Processor is capable of receiving all eight Omega channels on 10.2 KHz. Diurnal recordings of selected station pairs made during the period October-November 1976 demonstrate the receiver performance and illustrate limitations for navigation using diurnal corrections.

- 43 DEMONSTRATION PROGRAM FOR OMEGA RECEIVER PROTOTYPE MICRO-COMPUTER DATA PROCESSING
R. W. Lilley, November 1976.

Using the prototype Omega receiver developed for the NASA Joint University Program plus a digital interface to a commercial microcomputer, a software routine to demonstrate receiver operation is described.

- 44 AN ASSEMBLER FOR THE MOS TECHNOLOGY 6502 MICROPROCESSOR AS IMPLEMENTED IN JOLT (TM) AND KIM-1 (TM)
Robert W. Lilley, November 1976.

The 6502 Assembler implemented at Ohio University for support of microprocessor program development in the Tri-University Program is described.

- 45 INTERACTIVE OMEGA PROPAGATION CORRECTIONS
Robert W. Lilley, January 1977.

An implementation of Coast Guard computer programs for Omega propagation corrections is described.

- 46 ANALYSIS OF A FIRST ORDER PHASE LOCKED LOOP IN THE PRESENCE OF GAUSSIAN NOISE
Paul R. Blasche, March 1977.

A first-order digital phase-locked loop is analyzed by application of a Markov chain model. Steady-state loop error probabilities, phase standard deviation and mean loop transient times are determined for various input signal-to-noise ratios. In addition, results for direct loop simulation are presented for comparison.

- 47 A MICROCOMPUTER-BASED LOW-COST OMEGA SENSOR PROCESSOR
Richard J. Salter, Jr., February 1977, Master's Thesis.

- 48 MINI-L LORAN-C RECEIVER
R. W. Burhans, March 1977.

A low-cost prototype Loran-C receiver front-end has been designed and bench-tested. This receiver concept provides outputs to interface with a microcomputer system. The development of sensor and navigation software for use with the Mini-L system is underway.

- 49 SIMULATION OF DIGITAL PHASE-LOCKED LOOPS
Paul R. Blasche, April 1977.

This technical memorandum deals with development of simulation equations for first- and second-order digital phase-locked loops. In addition, examples of loop simulation are given to determine loop performance with respect to several loop parameters.

- 50 A KEYBOARD INTERFACE FOR THE JOLT MICROPROCESSOR
Lee Wright, May 1977.

The Ohio University Microprocessor Navigation Receiver Base utilizes the JOLT(TM) microcomputer. This keyboard interface is designed to allow data input without use of a teleprinter.

- 51 A FOUR DIGIT MEMORY-MAPPED DISPLAY
Ralph E. Smith, May 1977.

An interface board has been fabricated for the Ohio University Microcomputer-Based Navigation Receiver to display data from the microprocessor.

- 52 INTERACTIVE LORAN-C-TO-GEOGRAPHIC AND GEOGRAPHIC-TO-LORAN-C
COMPUTATION
Lynn M. Piecuch and Robert W. Lilley, August 1977.

An implementation of Naval Oceanographic Office computer software for Loran-C is presented.

- 53 CIRCUIT METHODS FOR VLF ANTENNA COUPLERS
R. W. Burhans, September 1977.

A summary of E-field antenna preamplifiers developed during the course of the NASA Tri-University Program studies on VLF methods for general aviation is presented. The circuit techniques provide useful alternative methods for Loran-Omega receiver system designers.

- 54 LORAN-C DIGITAL WORD GENERATOR FOR USE WITH A KIM-1 MICRO-
PROCESSOR SYSTEM
James D. Nickum, December 1977.

The digital word generator used with Mini-L front end to develop a Loran sensor processor at Ohio University is described.

- 55 MICROPROCESSOR-TO-SYSTEM/370 INTERFACE
Robert W. Lilley, February 1978.

A hardware interface is described which allows direct memory load of a microprocessor from the host System/370 computer, eliminating paper tape handling.

- 56 STAND-ALONE DEVELOPMENT SYSTEM USING A KIM-1 MICROCOMPUTER
 MODULE
 James Nickum, March 1978.

Documentation of the stand-alone microprocessor development system used in the navigation sensor processor research at Ohio University is described.

- 57 A LOW-COST LORAN-C ENVELOPE PROCESSOR (The Mini-L Loran-C
 Receiver)
 R. W. Burhans, April 1978.

A reprint of published article on the Mini-L Loran-C receiver front-end is presented. Complete circuit details are given with a basic introduction to Loran-C navigation and time-frequency standard uses. The Mini-L concept is of particular interest to the low-budget experimenter as an RF signal interface for more sophisticated end use.

- 58 A VIDEO DISPLAY INTERFACE FOR THE LORAN-C NAVIGATION RECEIVER
 DEVELOPMENT SYSTEM
 Joseph P. Fischer and Robert W. Lilley, May 1978.

A character-mode video unit is described which allows microprocessor-controlled display of program and navigation data with a small investment in logic.

- 59 COMPUTING LORAN TIME DIFFERENCES WITH AN HP-25 HAND
 CALCULATOR
 Edwin D. Jones, August 1978.

Accurate Loran-C time differences can be calculated from known transmitter and receiver positions using the program described.

- 60 PHASE-LOCKED TRACKING LOOPS FOR LORAN-C
 R. W. Burhans, August 1978.

Two, portable, battery-operated Loran-C receivers have been fabricated to evaluate simple envelope detector methods with hybrid analog-digital phase-locked loop sensor processors. The receivers are being used to evaluate Loran-C in general aviation applications. Complete circuit details are given for the experimental sensor and readout system.

- 61 LORAN-C FLIGHT TEST SOFTWARE
 James D. Nickum, August 1978.

Described is the software package developed for the KIM-1 Micro-System and the Mini-L PLL receiver to simplify taking flight test data at Ohio University.

- 62 PREAMPLIFIER NOISE IN VLF RECEIVERS
R. W. Burhans, September 1978.

Rapid methods of estimating antenna preamplifier noise contribution to receiver performance are presented for JFET or CMOS transistors. An improved CMOS preamplifier circuit is suggested.

- 63 LORAN-C TIME DIFFERENCE CALCULATIONS
Joseph P. Fischer, October 1978.

A simplified approach to calculate Loran-C time differences from a given geographic location is presented.

- 64 INITIAL FLIGHT TEST OF A LORAN-C RECEIVER/DATA COLLECTION SYSTEM
Joseph P. Fischer and James D. Nickum, November 1978.

Described are the flight test results of a Loran-C navigation receiver/data collection system designed at Ohio University.

- 65 ACTIVE ANTENNA FOR THE VLF TO HF OBSERVER
R. W. Burhans, February 1979.

This report is a prepublication manuscript submitted to one of the contemporary electronics magazines as part of a series on VLF-LF signal reception problems. The report presents a simple and low-cost method of fabricating an active antenna preamplifier system covering the range of 10 KHz to 10 MHz, for use with tunable communications receivers. The same type of preamplifier system can be used with airborne VLF navigation receivers.

- 66 ANALYSIS AND DESIGN OF A SECOND-ORDER DIGITAL PHASE-LOCKED LOOP
Paul R. Blasche, March 1979.

A second-order digital phase-locked loop is analyzed by application of a Markov chain model with alternatives. Steady-state loop error statistics and mean transient time are determined for various loop parameters. In addition, a hardware digital phase-locked loop was constructed and tested to demonstrate the applicability of the Markov chain mode.

- 67 LORAN-C FLIGHT DATA BASE
Robert W. Lilley, February 1979.

A large file of Loran-C data to be used in receiver design and testing is documented.

- 68 RESULTS OF THE SECOND FLIGHT TEST OF THE LORAN-C RECEIVER/DATA COLLECTION SYSTEM
Joseph P. Fischer, March 1979.

Reported are the results of a second flight test of the

Loran-C system under development at Ohio University using a variation of the techniques used for the first flight test.

- 69 DIGITAL PHASE-LOCKED LOOP DEVELOPMENT AND APPLICATION TO LORAN-C
Daryl L. McCall, September 1979.

A digital phase-locked loop has been developed and implemented for use in a low-cost Loran-C receiver. This paper documents the DPLL design and application to Loran-C.

- 70 ACTIVE ANTENNA COUPLER FOR VLF
R. W. Burhans, November 1979.

A reprint of a paper published in the "Ham Radio Magazine", Volume 12, Number 10, October 1979, is presented. The circuit designs are applicable to a variety of VLF-HF active antenna receiving systems including Omega and Loran-C for airborne and marine users.

- 71 EXPERIMENTAL LOOP ANTENNAS FOR 60 KHz to 200 KHz
R. W. Burhans, December 1979.

A series of loop antennas have been fabricated and evaluated for possible use with Loran-C and other VLF to LF band receivers. A companion low noise and very high gain preamplifier circuit has been devised to operate the loop antennas remote from the receiver. Further work is suggested on the multiple loop antenna systems to provide omni-directional coverage and reduce E-field noise pickup in navigation or communications systems.

- 72 DATA REDUCTION SOFTWARE FOR LORAN-C FLIGHT TEST EVALUATION
Joseph P. Fischer, December 1979.

This paper describes a set of programs written for use on Ohio University's 370 computer for reducing and analyzing flight test data.

- 73 LORAN DIGITAL PHASE-LOCKED LOOP AND RF FRONT-END SYSTEM ERROR ANALYSIS
Daryl L. McCall, December 1979.

Various experiments have been performed to determine the system error of the DPLLs and RF front-end currently being used in a Loran receiver prototype. This paper documents those experiments and their results.

- 74 RESULTS OF A LORAN-C FLIGHT TEST USING AN ABSOLUTE DATA REFERENCE
Joseph P. Fischer, January 1980.

The results of a flight test using the Loran-C receiver and data collection system developed at Ohio University are described in this paper. An absolute data reference was

provided by the Lincoln Laboratories DABS (Discrete Address Beacon System) facility.

- 75 ANALYSIS OF FIRST AND SECOND ORDER BINARY QUANTIZED DIGITAL PHASE-LOCKED LOOPS FOR IDEAL AND WHITE GAUSSIAN NOISE INPUTS
Paul R. Blasche, March 1980. (Dissertation)

Specific configurations of first and second order all digital phase-locked loops are analyzed for both ideal and additive white gaussian noise inputs. In addition, a design for a hardware digital phase-locked loop capable of either first or second order operation is presented along with appropriate experimental data obtained from testing of the hardware loop. All parameters chosen for the analysis and the design of the digital phase-locked loop are consistent with an application to an Omega navigation receiver although neither the analysis nor the design is limited to this application.

- 76 DC-TO-DC POWER SUPPLY FOR LIGHT AIRCRAFT FLIGHT TESTING
Stephen R. Yost, December 1980.

A DC-to-DC power supply has been designed and fabricated to operate the prototype Loran-C receiver and data collection system currently in use at Ohio University. The supply is designed to operate from an aircraft electrical system.

- 77 BI-DIRECTIONAL COMMUNICATION INTERFACE FOR MICROPROCESSOR-TO-SYSTEM/370
Joseph P. Fischer, January 1981.

Described is a hardware and software interface to allow two-way communication between a microprocessor system and the IBM System/370.

- 78 LORAN-C PLOTTING PROGRAM FOR PLOTTING LINES OF POSITION ON STANDARD CHARTS
James P. Roman, February 1981.

The Loran-C plotting program was designed to plot Loran-C lines of position on any standard chart and is used in the data-collection system currently in use at Ohio University Avionics Engineering Center.

- 79 AUTOMATIC GAIN CONTROL
James P. Roman, March 1981.

An automatic gain control has been designed and fabricated to operate with the Loran-C prototype receiver and data-collection system currently in use at Ohio University.

- 80 A LORAN-C PROTOTYPE NAVIGATION RECEIVER FOR GENERAL AVIATION
Robert W. Lilley and Daryl L. McCall, August 1981.

The design, fabrication and evaluation of a prototype Loran-C receiver is described. Hardware is complete and microcomputer programming continues for addition of area-navigation

capability. The receiver is an envelope-processor, offering simplicity of RF processor circuitry.

- 81 **COMMUTATED AUTOMATIC GAIN CONTROL SYSTEM**
 Stephen R. Yost, November 1981

A commutated AGC system for the Ohio University prototype Loran-C receiver is described. The circuit design, fabrication, and test results are presented in this paper.

- 82 **A PROTOTYPE INTERFACE UNIT FOR MICROPROCESSOR-BASED NAVIGATION SYSTEM**
 Stanley M. Novacki III, November 1981

A command entry and display device designed to allow convenient operation of the Loran-C receiver-processor is described.

TECHNICAL MEMORANDUM OU NASA 77

BI-DIRECTIONAL COMMUNICATION INTERFACE
FOR MICROPROCESSOR-TO-SYSTEM/370

Described is a hardware and software interface
to allow two-way communication between a
microprocessor system and the IBM System/370

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I. INTRODUCTION

This paper documents the design and operation of a bi-directional communication interface between a microcomputer and the IBM System/370. The hardware unit inter-connects a modem to interface to the S/370, the microcomputer with an EIA I/O port, and a terminal for sending and receiving data from either the microcomputer or the S/370. Also described is the software necessary for the two-way interface. This interface has been designed so that no modifications need to be made to the terminal, modem, or microcomputer. This unit is designed to upgrade a uni-directional interface already in use [1]

II. INTERFACE DESCRIPTION: HARDWARE

Figure 1 shows the paths of signals between the microcomputer, the modem, and the terminal. The hardware interface consists of a four-pole, three-position switch and cables and plugs to connect the switch box to the other devices. All signals are assumed to be RS-232C (EIA standard).

In switch position 1, the microcomputer is connected directly to the terminal; all communications are between these two only. The modem is isolated in this position and it is not necessary to have it connected if no communication to the S/370 is desired. In position 2, the serial out from the keyboard is routed to the modem for communicating to the S/370. The serial out from the modem goes to the terminal and the serial in of the microcomputer. In this position, it is possible to send commands and receive responses from the S/370, while the microcomputer reads the data sent by the S/370. Thus it is possible to load a program into the microcomputer by displaying the object file on terminal. It is necessary to switch to position 1 and issue the microcomputer load command prior to typing the file. Position 3 on the switch box connects the serial out from the modem to the terminal and to the serial in on the microcomputer. In addition, the serial out from the microcomputer is sent to the modem. Here, the microcomputer communicates directly with the S/370, the terminal always displays the response sent by the S/370. With proper positioning of the half-duplex/full-duplex switches on the terminal and modem, the responses from the microcomputer may also be displayed. Note that the serial-out from the terminal is isolated, thus it may be necessary to start a program on the microcomputer by pressing the NMI (non-maskable interrupt) switch on the switch box.

Table 1 lists the connection used on the terminal and modem. Connections for RS-232C are made through 25-pin D-connectors. Data terminal equipment (DTE) devices are supplied with a male (DB-25P) connector while data communication equipment (DCE) devices are supplied with a female (DB-25S) connector. Figure 2 shows the detailed routing of connections from the connectors on the terminal and modem through the switch box.

III. INTERFACE DESCRIPTION: SOFTWARE

Full utilization of the bi-directional interface requires a set of programs to be run simultaneously on the microcomputer and the S/370. Figure 3 shows a block diagram of how the programs would operate for a typical application. Some points to be considered in writing the interface software are:

- a. Most microcomputers store character data internally as ASCII.
- b. Serial communications between devices are generally in ASCII format.
- c. The I/O routines for the S/370 expect to receive ASCII which is then converted to EBCDIC, which the S/370 uses for internal storage of character data.
- d. The Conversational Monitor System (CMS) portion of the VM/370 operating system is line-oriented, i.e., no system action is taken until a carriage return (hex OD) is received.
- e. The S/370 issues a prompt when ready for another line.

A typical application for which this interface has been used is transmitting data collected by the microcomputer on a cassette tape to the S/370, where it is stored on a disk file for further processing. The sequence of events is as follows: the data to be transmitted is stored in a buffer in the microcomputer's memory. Generally, 80 characters comprise one line. Note that one byte consists of two four-bit hexadecimal numbers, each of which is converted to ASCII. Thus if 80 characters are to be sent, the buffer is 40 bytes long. After 80 characters are sent, a carriage return (hex OD) is sent. The S/370 does the ASCII-to-EBCDIC conversion and places the EBCDIC characters in a user buffer in the S/370 memory. When the S/370 is ready to receive another line, it sends a series of control characters. The microcomputer reads and recognizes these control characters as the prompt signal to send another line. The sequence of control characters currently sent by S/370 is shown in Figure 4.

Appendix A gives a listing of a MOS Technology 6502 microcomputer program (intended to be run using the 'Super-Jolt' micro unit) for reading 40 bytes of data from a Memodyne digital cassette tape unit and sending these to the S/370. The data to be sent are packed BCD numbers; i.e., one BCD digit occupies four bits, two BCD numbers are contained in one byte. Each BCD digit is sent as ASCII by the 'output byte' routine in the microcomputer monitor program (at address 72B1 (hex) in the Super-Jolt (TM) monitor). A carriage return is sent at the end of the line with a call to the WRT routine at address 72C6 (hex).

Program lines 1 to 78 are initialization steps used for the Memodyne interface hardware and to position the tape properly. Lines 79 to 91 constitute the main part of the program which builds up the 40-byte buffer then sends the buffer to the S/370. This part loops continuously whether or not any data is received. The operator should monitor the operation to stop the program when all the data has been transmitted. Subroutine READ is called to read a byte from the tape unit. Subroutine W370 sends the 40-character buffer to the S/370, sends a carriage return, then looks for a period (hex 2E) followed by a DC-1 (hex 11). If this sequence is not done, the S/370 issues a read-error message. When these two characters are received, control is passed back to the main program sequence.

Subroutine RDT is a modification of the RDT routine at address 72E9 in the Jolt monitor. Most serial-read routines on microcomputers are full-duplex; as each bit is received, it is echoed back out to the sending device. However, the S/370 can receive half-duplex only. Thus it is necessary to change the interface method through the modem or to re-write the read routine so that the received bits are not echoed by the microcomputer. This is the purpose of having a separate read routine. If this is not done, read-errors result. The program presented here is shown to illustrate one application of the bi-directional interface. Other uses on other microcomputers would still use the same basic philosophy.

The companion program that is run on the S/370 is shown in Appendix B. This program is written in IBM 360/370 assembler language [2] using standard CMS I/O routines. Again this program illustrates the application of sending data to the S/370 for storage on a disk file.

The data is read 80 bytes at a time, each BCD character in its ASCII format. Each character read is stripped of the upper four-digit mask and is repacked. This is done by the translate instruction at line 88 and the PACK instruction at line 90. Since one record produces only 40 packed BCD digits, two lines are read before one 80-byte record is written to the file. A blank line or an incomplete line is filled to the end with zeros. Each time a record is written, a counter is incremented which is printed at the end of program execution.

IV. INTERFACE OPERATION

The example of transmitting data from the microcomputer to the S/370 will be continued here to show how the interface may be operated. After the interface is properly connected, power should be applied to all units. At this point it is usually necessary to load the microcomputer with a program stored on a disk file. Thus the switch box should be set to position 2 and the appropriate CMS LOGON procedure performed. When the microprocessor object code is ready for transmittal (through editing, assembling, simulating, etc.) the switch box should be set to position 1, the microcomputer reset button pushed, and a carriage return or other appropriate

key to reset the microcomputer typed. Then issue the proper command to set the microcomputer for loading hexadecimal data over its serial lines. The switch box is then set back to position 2 and the appropriate command is issued to the S/370 to load the microcomputer with the object file. Next, the unit is switched back to position 1 to verify correct loading, initialize any memory locations and set up the NMI vector address to the start of the program. Now the switch box is placed in position 2 and the program to receive the data is started and then the unit is set to position 3 and the NMI button pressed.

As operation commences, the prompting period and any other responses from the S/370 will be displayed on the terminal. Depending on the setting of the half-duplex/full-duplex switches on the terminal and modem, data sent by the microcomputer will also be displayed on the terminal.

When the operation is finished, the unit may be set to position 2 to stop the S/370 program then position 1 to stop the microcomputer program.

V. SUMMARY

A discussion was presented here of an interface unit and software procedures to allow two-way communication between a microcomputer and a central computer. This can be used for two-way data transmission, control and other applications where bi-directional communications are necessary. As an aid to setting up the software for other computer systems, ASCII [3] and EBCDIC [4] tables are given in Tables 2 and 3.

VI. REFERENCES

- [1] Lilley, Robert W., *Microprocessor-to-System/370 Interface*, OU NASA TM-55 (Revised), Avionics Engineering Center, Department of Electrical Engineering, Ohio University, April, 1978.
- [2] OS/VS - DOS/VS - VM/370 Assembler Language, GC33-4010-4, International Business Machines Corporation, February, 1975.
- [3] Deem, Bill R., Kenneth Muchow, and Anthony Zeppa, "Digital Computer Circuits and Concepts", Reston Publishing Company, Inc., Reston Virginia, 1974, pg. 56.
- [4] IBM System/370 Principles of Operation, GA22-7000-5, International Business Machines Corporation, August 1976, pg. 288.

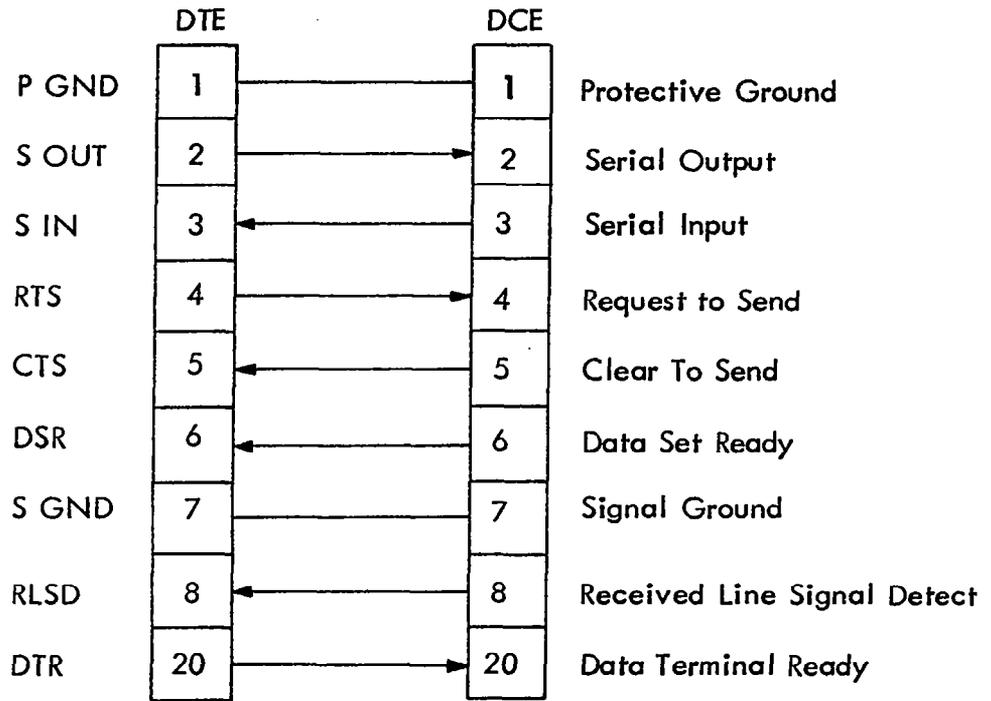


Table 1. RS-232C Connections.

	000	001	010	011	100	101	110	111
0000	NULL	① DC ₀	b	0	@	P	Unassigned	
0001	SOM	DC ₁	!	1	A	Q		
0010	EOA	DC ₂	"	2	B	R		
0011	EOM	DC ₃	#	3	C	S		
0100	EOT	DC ₄ (stop)	\$	4	D	T		
0101	WRU	ERR	%	5	E	U		
0110	RU	SYNC	&	6	F	V		
0111	BELL	LEM	'	7	G	W		
1000	FE ₀	S ₀	(8	H	X		
1001	HT / SK	S ₁)	9	I	Y		
1010	LF	S ₂	.	:	J	Z		
1011	V _{TAB}	S ₃	+	;	K	[
1100	FF	S ₄	(comma)	<	L	\		
1101	CR	S ₅	-	=	M]		
1110	SO	S ₆	.	>	N	↑		
1111	SI	S ₇	/	?	O	←		

ACK
②
ESC
DEL

Example:

100	0001
-----	------

 = A
b₇-----b₁

The abbreviations used in the figure mean:			
NULL	Null Idle	CR	Carriage return
SOM	Start of message	SO	Shift out
EOA	End of address	SI	Shift in
EOM	End of message	DC ₀	Device control ① Reserved for data Link escape
EOT	End of transmission	DC ₁ - DC ₃	Device control
WRU	"Who are you?"	ERR	Error
RU	"Are you . . . ?"	SYNC	Synchronous idle
BELL	Audible signal	LEM	Logical end of media
FE	Format effector	SO ₀ - SO ₇	Separator (information) Word separator (blank, normally non-printing)
HT	Horizontal tabulation	ACK	Acknowledge
SK	Skip (punched card)	②	Unassigned control
LF	Line feed	ESC	Escape
V/TAB	Vertical tabulation	DEL	Delete Idle
FF	Form feed		

Table 2. ASCII Table.

		00				01				10				11				Bit Positions 0,1	
		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11	Bit Positions 2,3	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	First Hexadecimal Digit	
Bit Positions 4, 5, 6, 7		[Zone Punched]																Zone Punched	
Second Hexadecimal Digit		[Zone Punched]																Zone Punched	
Digit Punched		[Zone Punched]																Digit Punched	
0000	0	NUL	DLE	DS		SP	&	.								0			
0001	1	SOH	DC1	SOS				/		~			A	J		1			
0010	2	STX	DC2	FS	SYN					b	k	v	B	K	S	2			
0011	3	ETX	TM							c	l	t	C	L	T	3			
0100	4	PF	RES	BYP	PN					d	m	u	D	M	U	4			
0101	5	HT	NL	LF	RS					e	n	v	E	N	V	5			
0110	6	LC	BS	ETB	UC					f	o	w	F	O	W	6			
0111	7	DEL	IL	ESC	EOT					g	p	x	G	P	X	7			
1000	8	GE	CAN							h	q	y	H	Q	Y	8			
1001	9	RLF	EM							i	r	z	I	R	Z	9			
1010	A	SMM	CC	SM		¢													
1011	B	VT	CU1	CU2	CU3	.	\$,	#										
1100	C	FF	IFS		DC4	<	-	%	@				¡		ª				
1101	D	CR	IGS	ENQ	NAK	()	_	'										
1110	E	SO	IRS	ACK		+	,	>	=				¥						
1111	F	SI	IUS	BEL	SUB	!	~	?	-									EO	
		[Zone Punched]																Zone Punched	
		[Zone Punched]																Zone Punched	

Card Hole Patterns

- | | | | |
|-----------------|--------------|---------|------------|
| ① 12-0-9-8-1 | ⑤ No Punches | ⑨ 12-0 | ⑬ 0-1 |
| ② 12-11-9-8-1 | ⑥ 12 | ⑩ 11-0 | ⑭ 11-0-9-1 |
| ③ 11-0-9-8-1 | ⑦ 11 | ⑪ 0-8-2 | ⑮ 12-11 |
| ④ 12-11-0-9-8-1 | ⑧ 12-11-0 | ⑫ 0 | |

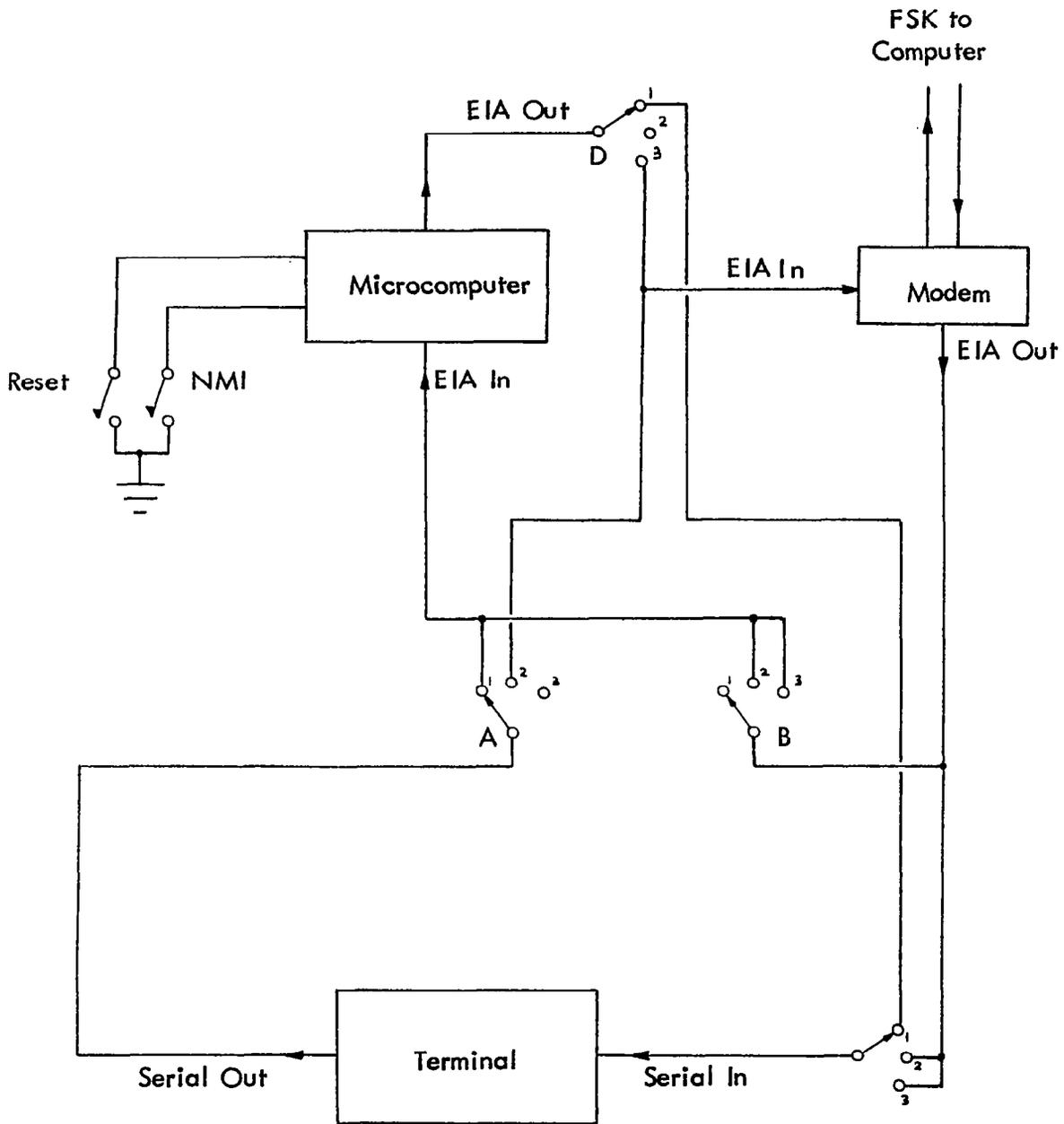
Control Character Representations

- | | | |
|----------------------|----------------------------------|-----------------------------|
| ACK Acknowledge | EOT End of Transmission | PF Punch Off |
| BEL Bell | ESC Escape | PN Punch On |
| BS Backspace | ETB End of Transmission Block | RES Restore |
| BYP Bypass | ETX End of Text | RLF Reverse Line Feed |
| CAN Cancel | FF Form Feed | RS Reader Stop |
| CC Cursor Control | FS Field Separator | SI Shift In |
| CR Carriage Return | GE Graphic Escape | SM Set Mode |
| CU1 Customer Use 1 | HT Horizontal Tab | SMM Start of Manual Message |
| CU2 Customer Use 2 | IFS Interchange File Separator | SO Shift Out |
| CU3 Customer Use 3 | IGS Interchange Group Separator | SOH Start of Heading |
| DC1 Device Control 1 | IL Interchange Link Separator | SOS Start of Significance |
| DC2 Device Control 2 | IRS Interchange Record Separator | SP Space |
| DC4 Device Control 4 | IUS Interchange Unit Separator | STX Start of Text |
| DEL Delete | LC Lower Case | SUB Substitute |
| DLE Data Link Escape | LF Line Feed | SYN Synchronous Idle |
| DS Digit Select | NAK Negative Acknowledgr | TA Tape Mark |
| EM End of Medium | NL New Line | UC Upper Case |
| ENQ Enquiry | NUL Null | VT Vertical Tab |
| EO Eight Ones | | |

Special Graphic Characters

- | | |
|-------------------------|-------------------------|
| ¢ Cent Sign | > Greater-than Sign |
| · Period, Decimal Point | ? Question Mark |
| < Less-than Sign | ˘ Grave Accent |
| (Left Parenthesis | ˆ Circumflex |
| + Plus Sign | ˜ Tilde |
| Logical OR | { Opening Brace |
| & Ampersand | } Closing Brace |
| ! Exclamation Point | ˆ^ Hat |
| \$ Dollar Sign | ˆ˘^ Fork |
| * Asterisk | ˆ˘˘ Closing Brace |
|) Right Parenthesis | ˆ˘˘˘ Long Vertical Mark |
| ˆ˘˘ Semicolon | |
| ˆ˘˘˘ Logical NOT | |
| - Minus Sign, Hyphen | |
| / Slash | |
| Vertical Line | |
| ˆ˘˘˘ Comma | |
| % Percent | |
| _ Underscore | |

Table 3. EBCDIC Table.



Note: Switches Shown in Position 1.

Figure 1. Signal Routing For Bi-Directional Interface.

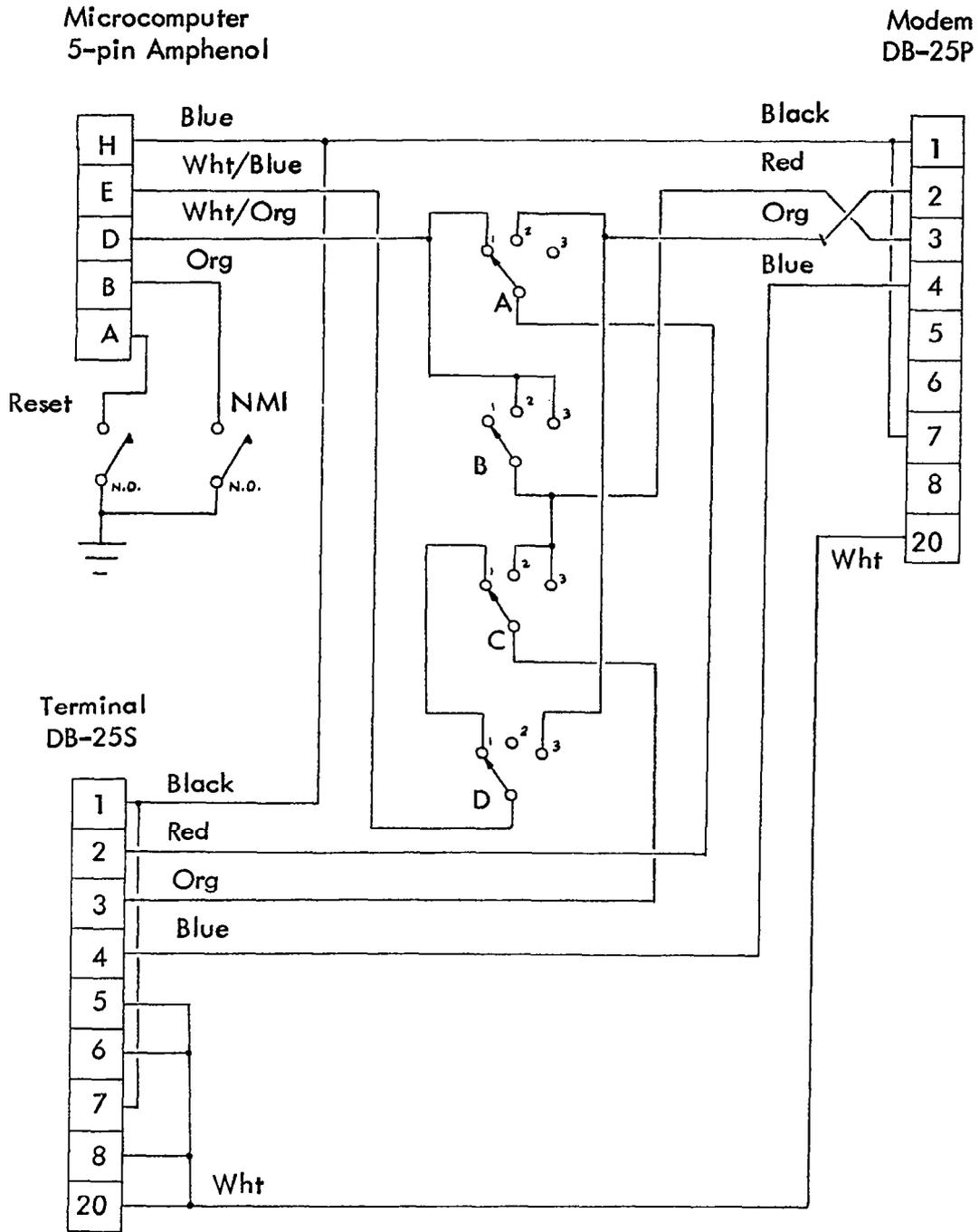


Figure 2. Interface Wiring Diagram.
(REVISED)

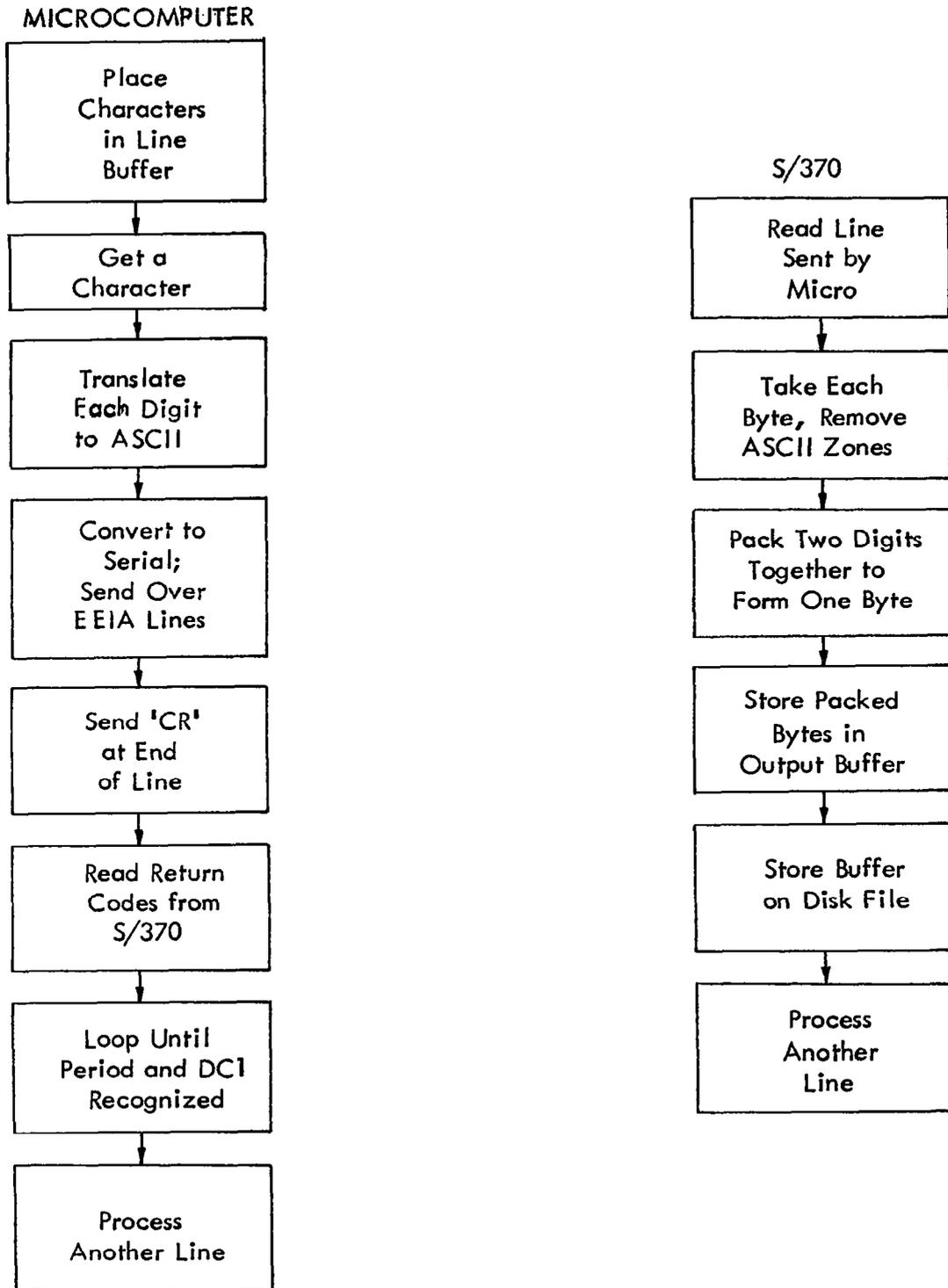


Figure 3. Control Program Flow Charts.

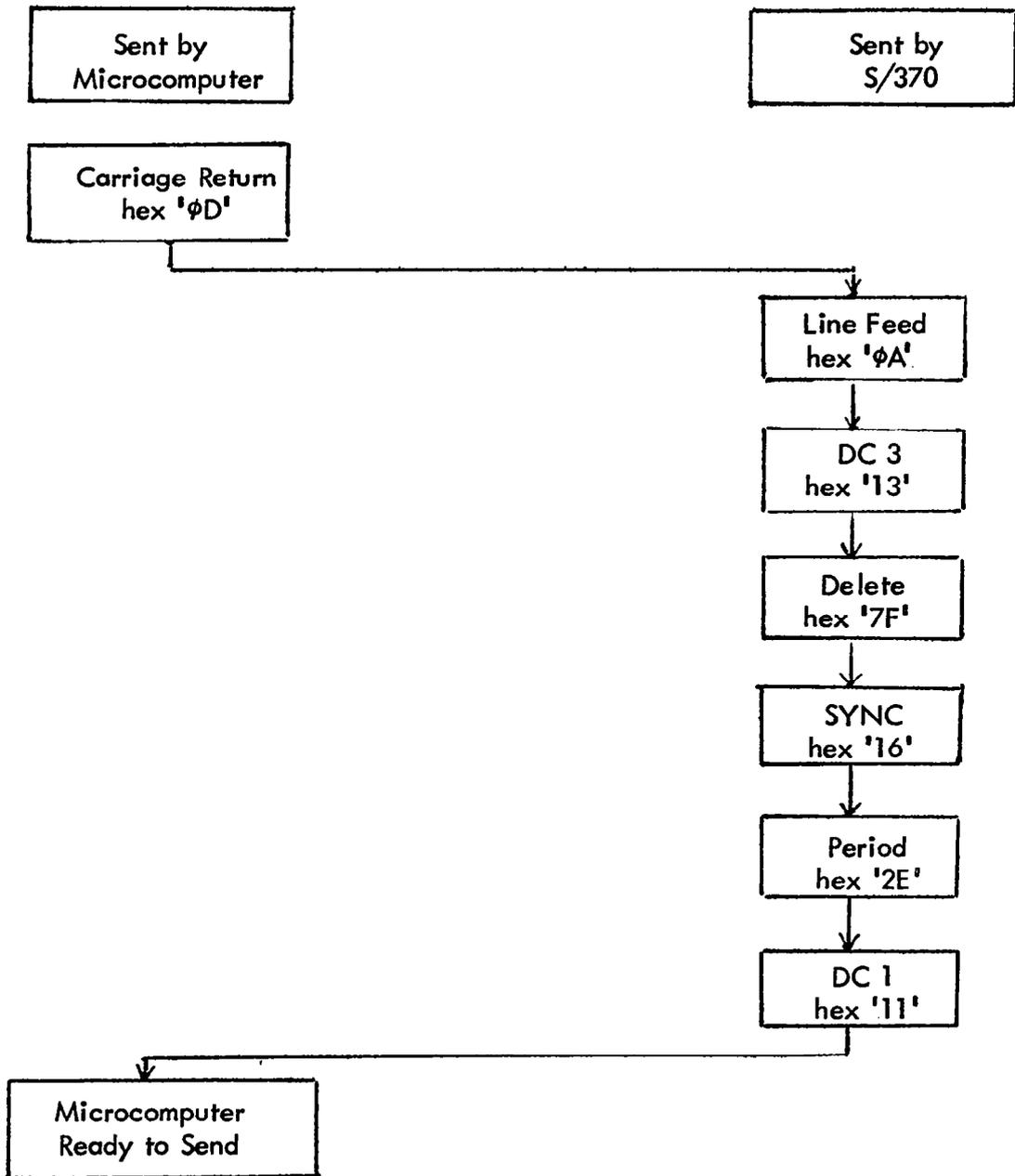


Figure 4. Control Characters Sent by S/370 After Receiving Carriage Return.

APPENDIX A. Program Listing for Microcomputer Control Program

FILE: UNLOAD S6502 A OHIO UNIVERSITY AVIONICS ENGINEERING CENTER

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***** UNL00010
* UNL00020
* THIS PROGRAM IS DESIGNED FOR RUNNING ON THE JOLT/MEMODYNE * UNL00030
* SYSTEM FOR RECOVERING DATA STORED ON THE DIGITAL TAPE. * UNL00040
* THE DATA IS READ IN 40 BYTES AT A TIME AND STORED IN A * UNL00050
* BUFFER. THEN THE BUFFER IS SENT TO THE S/370 OVER THE JOLT'S * UNL00060
* SERIAL LINES. WITH ASCII CONVERSION, 80 BYTES ARE ACTUALLY * UNL00070
* SENT OVER THE SERIAL LINES. * UNL00080
* * UNL00090
* J.P. FISCHER 08/1980 * UNL00100
* * UNL00110
***** UNL00120
* UNL00130
* UNL00140
PIAA EQU $4000 ADDRESS OF PIA SIDE A UNL00150
PIAB EQU $4002 ADDRESS OF PIA SIDE B UNL00160
WRT EQU $72C6 JOLT WRITE DATA TO SERIAL OUT LINE UNL00170
WROB EQU $72B1 UNL00180
MPB EQU $6E02 PIA B FOR SERIAL I/O WORK UNL00190
MCLK1T EQU $6E04 PIA TIMER UNL00200
MCLKRD EQU $6E04 SAME AS ABOVE UNL00210
MCLK1F EQU $6E05 SOME MORE TIMER STUFF UNL00220
MAJCRT EQU $EA UPPER 8 BITS OF BAUD RATE UNL00230
MINCRT EQU $EB LOWER 8 BITS OF BAUD RATE UNL00240
TAPESY EQU %00000010 PATTERN FOR TAPE SYNC CHECK UNL00250
BOT EQU %00000100 PATTERN FOR BOT/EOT CHECK UNL00260
LP EQU %00010000 PATTERN FOR LOAD FOWARD FUNCTION UNL00270
REW2 EQU %00100000 PATTERN FOR REWIND OPERATION UNL00280
START EQU %10000000 PATTERN FOR INITIATING STABT UNL00290
* UNL00300
ORG 0 UNL00310
XTEMP BSS 1 TEMPORARY FOR X UNL00320
YTEMP BSS 1 TEMPORARY FOR Y UNL00330
BUFFER BSS 40 UNL00340
* UNL00350
* UNL00360
ORG $200 UNL00370
JSR INIT SET UP PIA FOR MEMODYNE UNL00380
LDA PIAB PREPARE TO CHECK BOT UNL00390
AND =BOT SEE IF ON LEADER UNL00400
BNE NOTBOT IF NOT, THEN OK UNL00410
LDA PIAB GET SIDE B UNL00420
EOR =LF CLEAR LCAD FOWARD BIT UNL00430
ORA =START SET START BIT HIGH UNL00440
STA PIAB AND STORE TO LOAL FOWARD UNL00450
BTLOOP LDA PIAB GET STATUS UNL00460
AND =BOT SEE IF STILL ON LEADER UNL00470
BEQ BTLOOP CONTINUE TESTING UNTIL OFF UNL00480
LDA PIAB UNL00490
ORA =LF SET LOAD FOWARD HIGH UNL00500
STA PIAB AND REPIACE UNL00510
IDLOOP LDA PIAB UNL00520
AND =BOT NOW LOOP UNTIL AT READY POINT UNL00530
BNE LDLOOP KEEP GOING UNTIL ON HOLE UNL00540
LDA PIAB UNL00550

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      EOR =LF      SET LOAD FOWARD IOW TO MOVE      UNL00560
      STA PIAB    OFF OF HOLE                      UNL00570
TLOOP LDA PIAB    UNL00580
      AND =BOT    UNL00590
      BEQ TLOOP   UNL00600
      LDX =$80    TIMER ROUTINE                   UNL00610
TIMXT DEX        UNL00620
      BNE TIMXT   KEEP LOOPING UNTIL OUT          UNL00630
      ORA =LF     NOW RETURN LOAD FOWARD         UNL00640
      STA PIAB    HIGH, SHOULD BE OFF OF HOLE    UNL00650
NOTBOT LDA =0     CLEAR ACCUM. AND SET           UNL00660
      STA PIAA+1  UNL00670
      STA PIAB+1  UNL00680
      LDA =$F8    UNL00690
      STA PIAB    UNL00700
      LDA =0      UNL00710
      STA PIAA    UNL00720
      LDA =$FF    UNL00730
      STA PIAB+1  UNL00740
      STA PIAA+1  UNL00750
      LDA PIAB    UNL00760
      AND =%11110111 UNL00770
      STA PIAB    UNL00780
*
*           NOW INITIALIZE THE 370 AND START      UNL00790
*           SENDING DATA.                      UNL00800
*
*
LFLDS LDX =0     READ 40 CHARACTERS FROM TAPE     UNL00810
L80   JSR READ   GET A BYTE FROM RECORDER        UNL00820
      STA BUFFER,X SAVE IN OUTPUT BUFFER         UNL00830
      INX       DO ANOTHER ONE                   UNL00840
      CPX =40   DONE 40 BYTES YET?              UNL00850
      BNE L80   IF NOT, DO AGAIN                 UNL00860
      LDY =40   SEND THESE 40                   UNL00870
      JSR W370  SEND TO SYSTEM                   UNL00880
      JMP LFLDS UNL00890
*
*           INITIALIZATION FOR PIA                UNL00900
*
INIT  LDX =0     UNL00910
      STX PIAA+1 UNL00920
      STX PIAB+1 UNL00930
      STX PIAA   UNL00940
      LDA =$B8   UNL00950
      STA PIAB   UNL00960
      LDA =$FF   UNL00970
      STA PIAA+1 UNL00980
      STA PIAB+1 UNL00990
      LDA =0     UNL01000
      ORA =LF    UNL01010
      ORA =REW2  UNL01020
      STA PIAB   UNL01030
      RTS       UNL01040
*
*
*           UNL01050
*           UNL01060
*           UNL01070
*           UNL01080
*           UNL01090
*           UNL01100

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```

***** UNLO1110
* UNLO1120
* THIS IS THE READING PORTION OF THE PROGRAM TO RECOVER * UNLO1130
* DATA FROM THE RECORDER AND PLACE IN THE MICROCOMPUTER'S * UNLO1140
* MEMORY. * UNLO1150
* * UNLO1160
***** UNLO1170
* UNLO1180
* UNLO1190
READ LDA PIAB UNLO1200
ORA =START SET START HIGH UNLO1210
STA PIAB UNLO1220
RDLP LDA PIAB UNLO1230
AND =TAPESY WAIT UNTIL SYNC IS HIGH UNLO1240
BEQ RDLP UNLO1250
LDA PIAB UNLO1260
EOR =START SET START LOW AGAIN UNLO1270
STA PIAB UNLO1280
INLP1 LDA PIAB UNLO1290
AND =TAPESY WAIT UNTIL SYNC IS LOW UNLO1300
BNE INLP1 UNLO1310
LDA PIAA GET THE DATA FROM RECORDER UNLO1320
RTS UNLO1330
* UNLO1340
* UNLO1350
***** UNLO1360
* UNLO1370
* THIS SUBROUTINE OUTPUTS A LINE OF CHARACTERS TO THE S/370. * UNLO1380
* THE ADDRESS OF THE BUFFER IS IN PAGE ZERO AND IS * UNLO1390
* INDEXED BY THE X-REGISTER. THE LENGTH OF THE BUFFER * UNLO1400
* TO BE SENT IS CONTAINED IN THE Y-REGISTER. AFTER THE * UNLO1410
* BUFFER IS SENT, A 'CR' IS SENT THEN THE PROGRAM WAITS * UNLO1420
* FOR THE CONTROL CHARACTERS BETWEEN THE 'CR' AND PERIOD * UNLO1430
* TO BE SENT BACK, THEN WAITS FOR THE CONTROL * UNLO1440
* CHARACTER AFTER THE PERIOD INDICATING THE S/370 * UNLO1450
* IS IN THE READ STATE. * UNLO1460
* * UNLO1470
***** UNLO1480
* UNLO1490
W370 LDX =0 POINT TO FIRST CHARACTER UNLO1500
STX XTEMP ZERO X-TEMP SPACE UNLO1510
STY YTEMP SAVE LENGTH UNLO1520
WLOOP LDX XTEMP GET POINTER UNLO1530
LDA BUFFER,X GET A CHARACTER UNLO1540
JSR WROB SEND IT UNLO1550
INC XTEMP X+1 UNLO1560
DEC YTEMP LESS ONE CHARACTER UNLO1570
BNE WLOOP GO AGAIN IF NOT DONE UNLO1580
LDA =$D CARRIAGE RETURN UNLO1590
JSR WRT TELL 370 THIS IS END-OF-LINE UNLO1600
SCANP JSR RDT READ JUNK FROM SYSTEM UNLO1610
CMP =$2E PERIOD UNLO1620
BNE SCANP UNLO1630
JSR RDT LOOK FOR UNLO1640
CMP =$11 DC1 UNLO1650

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```

        BNE SCANP                                UNL01660
        RTS          RETURN TO CALLER            UNL01670
*
*
*
*****
*
*          HIGH SPEED REWIND.                    * UNL01710
*
*
*****
*
        JSR INIT                                UNL01740
        LDA =$B8                                UNL01750
        STA PIAB                                UNL01760
        LDA =LF                                  UNL01770
        STA PIAB                                UNL01780
        ORA =REW2                                UNL01780
        STA PIAB                                UNL01790
        BRK                                      UNL01800
*
*
*****
*
        MODIFIED JOLT READ ROUTINE.              * UNL01850
*          THIS ROUTINE IS IDENTICAL TO THE ORIGINAL 'RDT' ROUTINE * UNL01860
*          AT ADDRESS $72E9, BUT THIS ROUTINE OPERATES IN HALF-   * UNL01870
*          DUPLEX RATHER THAN FULL-DUPLEX MODE.                   * UNL01880
*
*
*****
*
RDT      LDX =8                                  UNL01890
*
RDT1     LDA MPB          WAIT FOR START BIT      * UNL01900
        LSR A
        BCC RDT1
*
*          JSR DLY1                                           UNL01910
*
RDT2     JSR DLY2
        LDA MPB          CY = NEXT BIT           UNL01920
        LSR A
*
*          PHP          SAVE BIT                               UNL01930
        TYA          Y CONTAINS CHAR BEING FORMED UNL01940
        LSR A
        PLP          RECALL BIT                       UNL01950
        BCC RDT4
        ORA =$80          ADD IN NEXT BIT            UNL01960
RDT4     TAY
        DEX
        BNE RDT2          LOOP FOR 8 BITS           UNL01970
        EOR =$FF          COMPLEMENT DATA          UNL01980
        AND =$7F          CLEAR PARITY              UNL01990
        JSR DLY2
        CLC
*
*
*****
*

```

DLY2	JSR DLY1		UNL02210
*			UNL02220
DLY1	PHA	SAVE FLAGS AND A	UNL02230
	PHP		UNL02240
	TXA		UNL02250
	PHA	SAVE X	UNL02260
	LDX MAJCRT		UNL02270
	LDA MINCRT		UNL02280
*			UNL02290
	STA MCLK1T		UNL02300
DL3	LDA MCLK1F		UNL02310
	BPL DL3		UNL02320
	DEX		UNL02330
	PHP		UNL02340
	LDA MCLKRD	RESET TIMER INT FLAG	UNL02350
	PLP		UNL02360
	BPL DL3		UNL02370
*			UNL02380
	PLA		UNL02390
	TAX		UNL02400
	PLP		UNL02410
	PLA		UNL02420
	RTS		UNL02430
*			UNL02440
*			UNL02450
	ORG \$FFFA		UNL02460
	HEX 00,02		UNL02470
*			UNL02480
	END		UNL02490

APPENDIX B. Program Listing for S/370 Control Program

FILE: UNLOAD\$\$ ASSEMBLE A

OHIO UNIVERSITY AVIONICS ENGINEERING CENTE

```

TITLE 'UNLOAD$$:  READS RECORDS FROM MEMODYNE/MICROCOMPUTER IN*UNL0001J
TERFACE AND STORES ON DISK.'                                UNL0002J
PRINT NOGEN                                                UNL0003J
SPACE                                                       UNL0004J
*****                                                    UNL0005J
*                                                           * UNL0006J
* THIS PROGRAM IS DESIGNED TO BE RUN ON THE S/370 IN CON- * UNL0007J
* JUNCTION WITH THE MICRO 'UNLOAD' PROGRAM AND THE MEMODYNE/ * UNL0008J
* MICROCOMPUTER HARDWARE INTERFACE.  RECORDS READ FROM * UNL0009J
* TAPE BE THE MICRO ARE SENT TO THE 370 IN ASCII, CP THEN * UNL0010J
* TRANSLATES THESE TO EBCDIC WHICH MUST BE TRANSLATED * UNL0011J
* BACK TO HEX BY THIS PROGRAM.  80 BYTES ARE SENT AT A * UNL0012J
* TIME (40 EQUIVALENT HEX CHARACTERS) AND 80 HEX CHARACTERS * UNL0013J
* ARE STORED ON THE DISK FILE.                               * UNL0014J
*                                                           * UNL0015J
* J. P. FISCHER      08/1980                                * UNL0016J
*                                                           * UNL0017J
*****                                                    UNL0018J
SPACE 2                                                    UNL0019J
UNLOAD$$ START X'E000'                                     UNL0020J
USING UNLOAD$$,12                                         UNL0021J
MVI  FLAGS,0      CLEAR ALL FLAG BITS                    UNL0022J
LA   1,8(,1)      POINT TO FILE NAME FIELD              UNL0023J
LR   2,1          SAVE PLIST ADDRESS                     UNL0024J
CLI  0(1),X'FF'   BLANK ?                               UNL0025J
BE   NOID         IF SO, ERROR                           UNL0026J
LA   1,8(,1)                                           UNL0027J
CLI  0(1),X'FF'   NO FILETYPE?                          UNL0028J
BE   NOID         IF NCT, ERROR                           UNL0029J
MVC  FILEID+8(16),0(2)  MOVE PARTIAL ID                  UNL0030J
LA   1,8(,1)                                           UNL0031J
CLI  0(1),X'FF'   NO FILEMODE                           UNL0032J
BE   NOMODE      IF NOT SUBSTITUTE 'A'                   UNL0033J
MVC  FILEID+24(2),16(2) MOVE IN NEW MODE                 UNL0034J
B    CHECK      CONTINUE                                UNL0035J
NOMODE MVI  FILEID+24,C'A' MOVE IN 'A'                   UNL0036J
MVI  FILEID+25,C' ' UNL0037J
SPACE 2 UNL0038J
CHECK  LA   1,8(,1) MOVE POINTER UP SOME MORE           UNL0039J
CLI  0(1),X'FF' SEE IF ANYTHING THERE                   UNL0040J
BE   CHECK1     IF NOT, CONTINUE                         UNL0041J
CLI  0(1),C'(' SEE IF OPTION                            UNL0042J
BNE  PARMERR    IF NOT, BAD PARM                        UNL0043J
LA   1,8(,1)    NEXT FIELD                              UNL0044J
CLI  0(1),X'FF' SEE IF BLANK                            UNL0045J
BE   CHECK1     UNL0046J
CLC  0(8,1),OPTREP SEE IF REPLACE OPTION                UNL0047J
BNE  BADOPT     IF NOT, CONTINUE                        UNL0048J
OI   FLAGS,1    SET REPLACE BIT                          UNL0049J
SPACE 2 UNL0050J
CHECK1 TM  FLAGS,1 SEE IF REPLACE IN EFFECT              UNL0051J
BZ   OPENF     IF NOT,GO ON                             UNL0052J
FSErase FSCB=FILEID UNL0053J
OPENF  FSOPEN FSCB=FILEID OPEN FOR WRITING              UNL0054J
CL    15,F36    SEE IF INVALID DISK                     UNL0055J

```

```

        BF      INVDISK                                UNL00560
        SPACE 2                                       UNL00570
*****
*
*           THIS PART OF THE PROGRAM CAUSES A TERMINAL      * UNL00580
*           READ TO GET THE ASCII CHARACTERS, THEN TRANSLATES * UNL00590
*           THEM TO HEX AND STORES ON DISK.                  * UNL00600
*                                                           * UNL00610
*                                                           * UNL00620
*                                                           * UNL00630
*****
        SPACE                                         UNL00640
        SLR    4,4                                     UNL00650
        SLR    7,7                                     UNL00660
        LA     2,WBUF      CLEAR RECORD COUNTER          UNL00670
        LA     4,8        WRITE BUFFER ADDRESS          UNL00680
        L      5,IBUF80   LOOP INCREMENT                UNL00690
RDLOOP  LA     3,IBUF     END OF LOOP                    UNL00700
        RDTERM IBUF      READ BUFFER ADDRESS            UNL00710
        LTR    0,0        GET A RECORD                  UNL00720
        BZ     DONE       SEE IF NULL LINE              UNL00730
        WAITT                                GO IF IT IS  UNL00740
        TR     IBUF(80),TRTBL  WAIT FOR I/O            UNL00750
        MVC    TEMP(8),0(3)  CHANGE TO HEX              UNL00760
STRIPZ  PACK   TEMP1(5),TEMP(9)  GET 8 ZONED BYTES      UNL00770
        MVC    0(4,2),TEMP1   REMOVE THE ZONES          UNL00780
        LA     2,4(2)       PUT PACKED CHARS. IN OUT BUFFER UNL00790
        BXLE  3,4,STRIPZ    NEXT POSITION IN OUTPUT BUFFER UNL00800
        SPACE                                         UNL00810
        RDTERM IBUF      CONTINUE UNTIL WHOLE RECORD DONE UNL00820
        LTR    0,0        GET ANOTHER 80 CHARS.         UNL00830
        BZ     DONE1      SEE IF NULL LINE              UNL00840
        WAITT                                GO IF IT IS  UNL00850
        LA     3,IBUF     WAIT FOR I/O                  UNL00860
        TR     IBUF(80),TRTBL  RE-INITIALIZE POINTER    UNL00870
Z1      MVC    TEMP(8),0(3)  GET 8 BYTES                UNL00880
        PACK   TEMP1(5),TEMP(9)  REMOVE ZONES          UNL00890
        MVC    0(4,2),TEMP1   PUT IN OUT BUFFER        UNL00900
        LA     2,4(2)       NEXT LOCATION              UNL00910
        BXLE  3,4,Z1       DO 80 BYTES                  UNL00920
        LA     2,WBUF     REINITIALIZE WRITE POINTER    UNL00930
        FSWRITE FSCB=FILEID  SEND TO DISK              UNL00940
        LTR    15,15      SEE IF ERROR                  UNL00950
        BNZ   WRERR      GO IF THERE IS                 UNL00960
        LA     7,1(7)     ADD ONE TO RECORD COUNT       UNL00970
        B     RDLOOP      PROCESS SOME MORE             UNL00980
        SPACE                                         UNL00990
DONE1   MVI    WBUF+40,0   PREPARE TO CLEAR              UNL01000
        MVC    WBUF+41(39),WBUF+40  REMAINING FIELD    UNL01010
        FSWRITE FSCB=FILEID  UNL01020
        LTR    15,15      UNL01030
        BNZ   WRERR      UNL01040
        LA     7,1(7)     ADD ONE TO RECORD COUNT       UNL01050
        SPACE                                         UNL01060
*****
*                                                           * UNL01070
*                                                           * UNL01080
*           NOW CLOSE THE FILE.                          * UNL01090
*                                                           * UNL01100

```

```

*
*****
* UNL0111J
* UNL0112J
* UNL0113J
* UNL0114J
* UNL0115J
* UNL0116J
* UNL0117J
* UNL0118J
* UNL0119J
* UNL0120J
* UNL0121J
* UNL0122J
* UNL0123J
* UNL0124J
* UNL0125J
* UNL0126J
* UNL0127J
* UNL0128J
* UNL0129J
* UNL0130J
* UNL0131J
* UNL0132J
* UNL0133J
* UNL0134J
* UNL0135J
* UNL0136J
* UNL0137J
* UNL0138J
* UNL0139J
* UNL0140J
* UNL0141J
* UNL0142J
* UNL0143J
* UNL0144J
* UNL0145J
* UNL0146J
* UNL0147J
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* UNL0153J
* UNL0154J
* UNL0155J
* UNL0156J
* UNL0157J
* UNL0158J
* UNL0159J
* UNL0160J
* UNL0161J
* UNL0162J
* UNL0163J
* UNL0164J
* UNL0165J
* UNL0166J
* UNL0167J
* UNL0168J
*
SPACE
PSCLOS# PSCB=FILEID CLOSE THE FILE
LINEDIT TEXT='..... RECORDS WRITTEN TO FILE.',
      SUB=(DEC,(7)),DOT=NO,RENT=NO
SLR 15,15 CLEAR RETURN CODE
BR 14 GO TO CMS
EJECT
NOID LINEDIT TEXT='DMSULD054E INCOMPLETE FILEID SPECIFIED.',
      DISP=ERRMSG,DOT=NO,RENT=NO
LA 15,24 RETURN CODE
BR 14 BACK TO CMS
SPACE
INVDISK LR 2,15 SAVE RETURN CODE
LINEDIT TEXT='DMSULD069E DISK '..' NOT ACCESSED.',
      SUB=(CHARA,FILEID+24),DISP=ERRMSG,DOT=NO,RENT=NO
LR 15,2 GET RETURN CODE
BR 14 BACK TO CMS
SPACE
WRTErr LR 2,15 SAVE RETURN CODE
LINEDIT TEXT='DMSULD105S ERROR '..' WRITING FILE '.....
..... ' ON DISK.',SUB=(DEC,(2),CHARA,FILEID+8,CHAR
A,FILEID+16,CHARA,FILEID+24),DISP=ERRMSG,
DOT=NO,RENT=NO
LA 15,100 RETURN CODE
BR 14 BACK TO CMS
SPACE
PARMERR LR 2,1 SAVE PARM ADDRESS
LINEDIT TEXT='DMSULD070E INVALID PARAMETER '..'',
      SUB=(CHARA,(2)),DISP=ERRMSG,DOT=NO,RENT=NO
LA 15,24 RETURN CODE
BR 14 BACK TO CMS
SPACE
BADOPT LR 2,1 SAVE OPTION ADDRESS
LINEDIT TEXT='DMSULD003E INVALID OPTION '..'',
      SUB=(CHARA,(2)),DISP=ERRMSG,DOT=NO,RENT=NO
LA 15,24 RETURN CODE
BR 14 BACK TO CMS
EJECT
DS 0D
F36 DC F'36'
IBUF80 DC AL4(IBUF+79)
OPTREP DC CL8'REP'
FILEID FSCB '* * *',BUFFER=WBUF,BSIZE=80
TEMP DS XL8
DC C'1'
TEMP1 DS XL5
FLAGS DS XL1
WBUF DS XL80
IBUF DS XL132
TBL DC X'00'
ORG TBL+8*16
DC XL16'00FABFBCFDFFFOFOFOFOFOFOFOFO'
ORG TBL+11*16
DC XL16'POF1P2P3P4P5P6P7P8P9FOFOFOFOFOFO'
TRTBL EQU TBL-X'40'
END UNLOAD$$

```

TECHNICAL MEMORANDUM OU NASA 78

LORAN-C PLOTTING PROGRAM FOR PLOTTING LINES
OF POSITION ON STANDARD CHARTS

The Loran-C plotting program was designed to plot Loran-C lines of position on any standard chart and is used in the data-collection system currently in use at Ohio University Avionics Engineering Center.

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I. INTRODUCTION

The NASA Tri-University program at Ohio University is currently involved in the development of a low-cost Loran-C navigation receiver for use in general aviation aircraft. This paper describes a set of programs designed to be run on the IBM System/370 computer at Ohio University. These programs are used to plot Loran-C lines of position (LOP) on any common map or standard aviation sectional chart. The Loran-C plotting program JRLOT FORTRAN uses a standard Calcomp-compatible plotting subroutine package for the Hewlett-Packard 7203A graphic plotter.

This paper gives a general description of the features of the Loran-C plotting program. This program involves a simple add/subtract method to calculate the LOP. Refer to Figure 1. Included is a description on how to use the program and some methods of operation.

II. FEATURES OF THE LORAN-C PLOTTING PROGRAM

The program will accommodate any scale of map desired. (Note: the larger the scale of the map the more distortion will occur.) The program was designed for standard aviation sectional charts; any larger scale than 1:500,000 is not recommended.

Plotting may be done on any size chart within the limitations of the Hewlett-Packard 7203A graphic plotter (10" high by 15" wide).

Four station pairs are calculated in the program's execution where, for the 9960 chain: (Master) control for W, X, Y, and Z is Seneca, NY 42° 42' 50.6"N and 76° 49' 33.9"W

Block address 1 is the W-pair
Caribou, ME 46° 48' 27.2"N and 67° 55' 37.7"W

Block address 2 is the X-pair
Nantucket, MA 41° 15' 11.9"N and 69° 58' 39.1"W

Block address 3 is the Y-pair
Carolina Beach, NC 34° 03' 46.0"N and 77° 54' 46.8"W

and block address 4 is the Z-pair
Dana, IN 39° 51' 07.5"N and 87° 29' 12.1"W

For best results only plot two LOP sets on a single chart.

The time difference for each line of position is placed to the top or side of the chart, depending on the angle of the LOP, along with the station pair identifier.

III. ACCURACY

There are two sources of error in the system. Although the latitude/longitude conversion subprogram takes into account the curvature of the earth, the plotting routine is purely linear, therefore, the larger the scale of the chart the greater the percentage of error. The error for large scale sectionals is approximately $\pm 10 \mu\text{sec}$. The error for small scale geographic survey charts is $\pm 5 \mu\text{sec}$. The other source of error is in measurement of the parameters listed below. These errors can be reduced by methods listed in Section IV depending on the accuracy the programmer wishes to achieve.

IV. EXECUTION

1. The center point of the chart must be measured as accurately as possible. Then, the latitude and longitude must be taken from that point. The proper form for entering into the computer is:

integer degrees integer minutes floating point seconds
###space##space##.#

2. Then measure the number of inches per degree of latitude and measure the number of inches per degree of longitude. See Figure 2.

3. Then enter the increment that the lines of position should be spaced apart.

Recommended increments are:

50.0 for standard sectional charts

2.0 for geographic survey charts.

4. Enter the actual dimensions of the chart to be plotted (see Figure 2). The chart should be no larger than 11 x 15 inches and no smaller than 5 x 5 inches. These are the practical limitations of the Hewlett-Packard 7203A plotter. When the program is finished executing, the chains will be located as follows:

Block Address	Station Pair
1	W
2	X
3	Y
4	Z

It is recommended to plot all four chains on a blank sheet of paper the same size as the chart.

V. IMPROVING ACCURACY

This procedure should be necessary only when there is a need for extreme accuracy. To make the Loran-C plotting program more accurate, three time difference positions are needed before execution of the program: the time difference of the center point, the time differences for a point left of center, and the time differences for a point right of center. Then it is a simple matter to align the grid with the known time-difference positions. By adding or subtracting from the latitude position of the center point, the grid will shift north or south respectively. By adding or subtracting from the longitude center point position, the grid will shift west or east respectively. Another method of adjusting the grid would be to add or subtract from the inches per degree parameters. Then the grid may be expanded or contracted respectively.

VI. SUMMARY

The Loran-C plotting program is a system of plotting routines and conversion subprograms. The program is designed to accommodate a wide range of mapping needs. The program may be easily modified to meet the specific needs of the current experiment.

VII. ACKNOWLEDGEMENTS

The subprogram TDPOS is a program written by Joseph P. Fischer of the Ohio University Avionics Engineering Center. The program was originally written for use in Loran-C data reduction. The subprogram TDS is a modification of a program also written by Mr. Fischer. This work is supported by the National Aeronautics and Space Administration.

VIII. BIBLIOGRAPHY

Loran-C User Handbook, United States Coast Guard, May 1980.

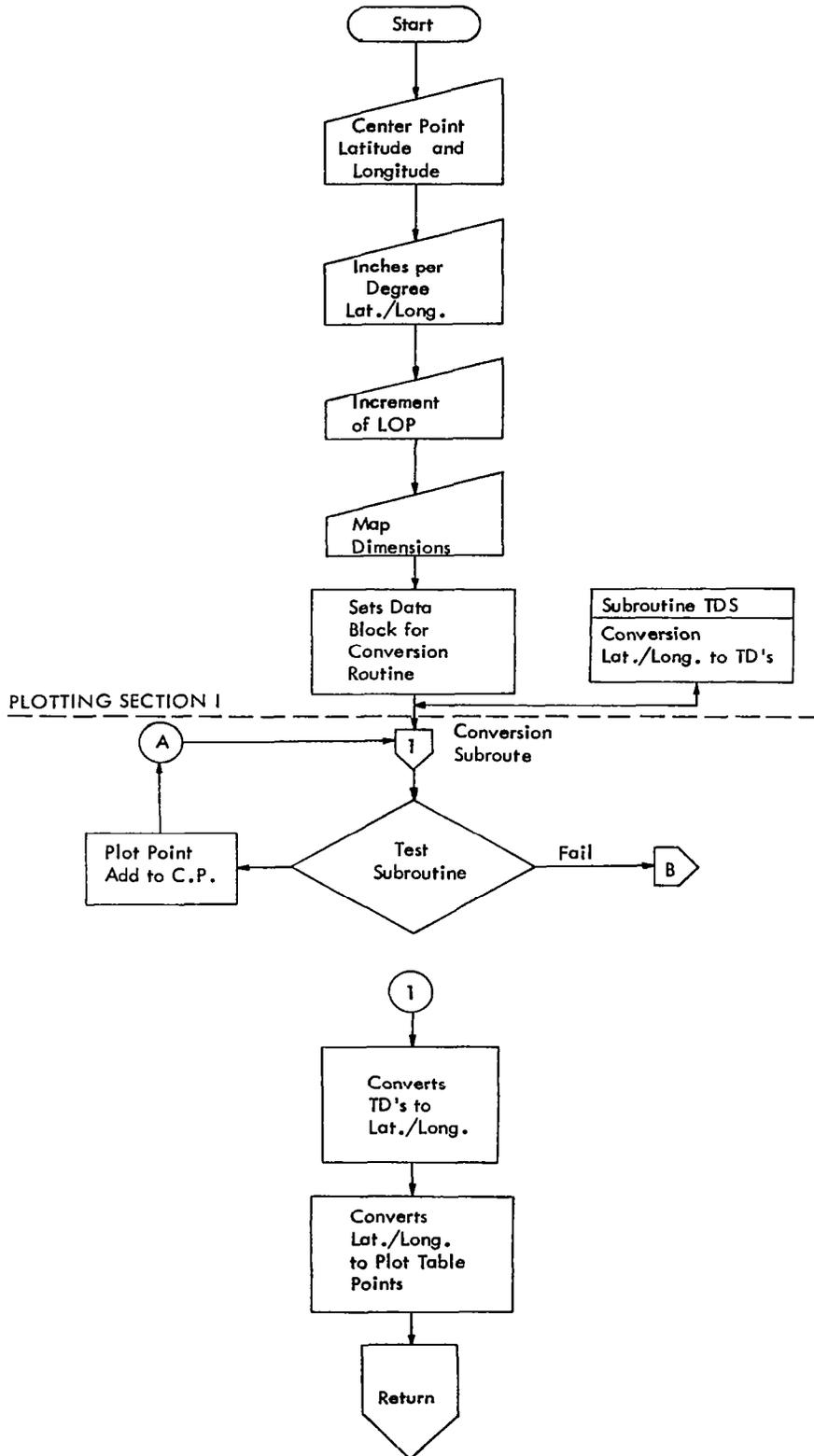


Figure 1. Flow Chart.

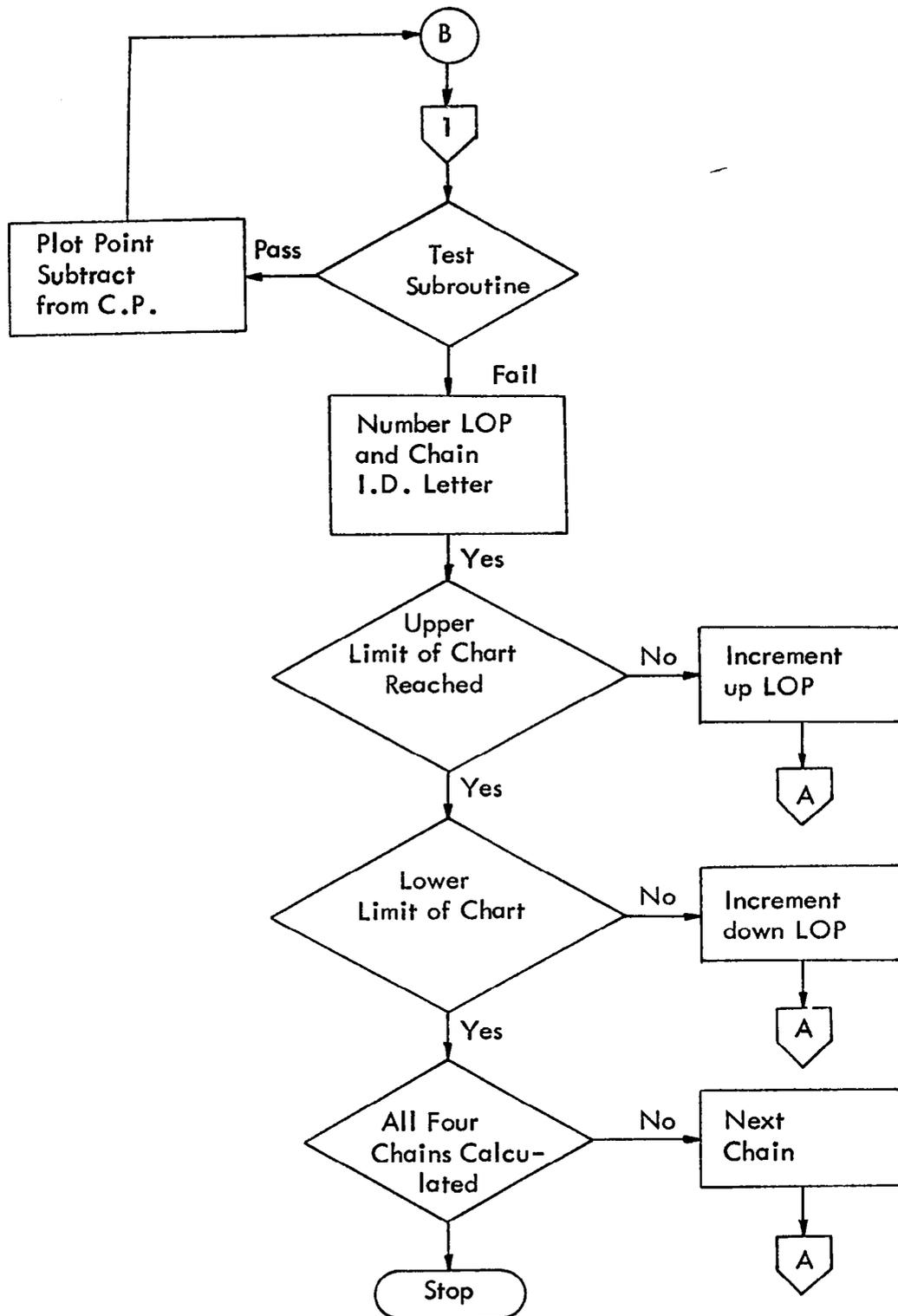


Figure 1. (Continued).

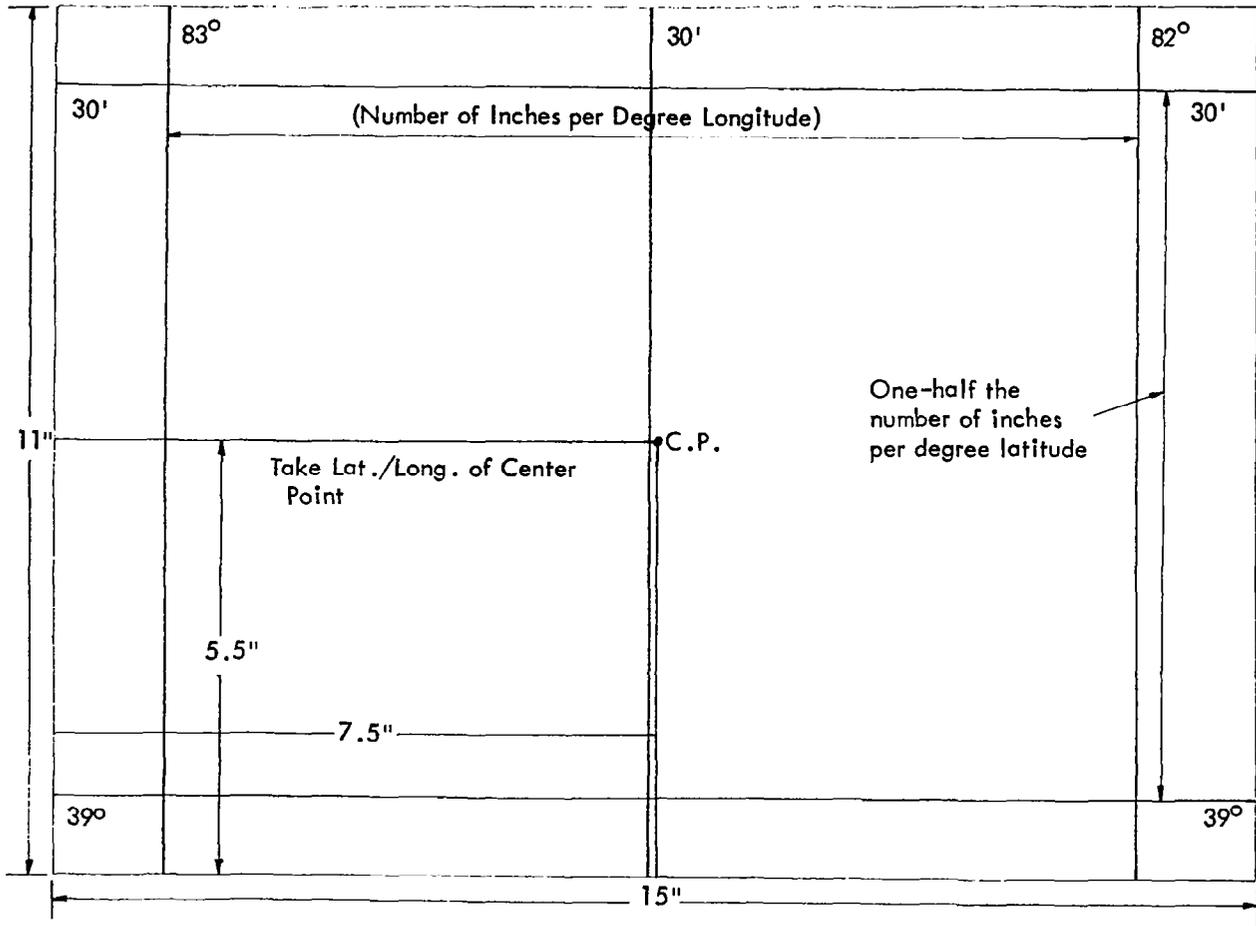


Figure 2. Sample Chart for Measurements.

APPENDIX A. Listing of JRPL0T Program

FILE: JRPL0T FORTRAN C

OHIO UNIVERSITY AVIONICS ENGINEERING CENTER

```

CCCCCCCCCCCCCCCC PLOTTING LORAN-C CURVES ON SECTIONAL CHARTS CCCCCC      JRP00010
  DIMENSION TD(4),TH(4),DRPOS(2),POS(2)                                JRP00020
  DIMENSION IBCD(2),X2(2,200),Y2(2,200)                              JRP00030
  DIMENSION BUF(1)                                                    JRP00040
  REAL*8 PHIR,GAMR                                                    JRP00050
  COMMON PHIR,GAMR                                                    JRP00060
  COMMON/CHAIND/DEL(2),A5,A6,AD(8),DM(8),CS(8)                        JRP00070
CCCCCCCCCCCCCCCCCCCC INPUT SECTION CCCCCCCCCCCCCCCCCCCCCCCCCCCCCC JRP00080
  WRITE(6,11)                                                           JRP00090
11  FORMAT('+','ENTER LATITUDE OF CENTER POINT FORM ### ## ##.# ') JRP00100
  READ(5,4) IDEG,MIN,SEC                                              JRP00110
  WRITE(6,12)                                                           JRP00120
12  FORMAT(' ','ENTER LONGITUDE OF CENTER POINT')                   JRP00130
  READ(5,4) IDEG1,MIN1,SEC1                                           JRP00140
4   FORMAT(I3,I2,I2,I2,F3.1)                                          JRP00150
  WRITE(6,13)                                                           JRP00160
13  FORMAT(' ','ENTER NUMBER OF INCHES PER DEGREE LATITUDE')       JRP00170
  READ(5,5)A                                                            JRP00180
  WRITE(6,14)                                                           JRP00190
14  FORMAT(' ','ENTER NUMBER OF INCHES PER DEGREE LONGITUDE')      JRP00200
  READ(5,5)B                                                            JRP00210
5   FORMAT(F7.4)                                                       JRP00220
  WRITE(6,15)                                                           JRP00230
15  FORMAT('+','INPUT INCREMENT BETWEEN L.O.P..')                   JRP00240
  READ(5,5)XINC                                                         JRP00250
  XINC2=XINC                                                            JRP00260
  IF(XINC.GT.10.0)XINC2=10.0                                          JRP00270
  B=B*(-1.0)                                                            JRP00280
  YIP=IDEG+(MIN+SEC/60.0)/60.0                                        JRP00290
  XIPI=IDEG1+(MIN1+SEC1/60.0)/60.0                                    JRP00300
  CALL PLOTS(BUF,1,11)                                                 JRP00310
CCCCCCCCCCCCCCCCCCCC MAP DIMENSIONS CCCCCCCCCCCCCCCCCCCCCCCCCCCCCC JRP00320
  WRITE(6,1)                                                            JRP00330
1   FORMAT('+','ENTER HORIZONTAL DIMENSION')                          JRP00340
  READ(5,2)XLAT                                                         JRP00350
2   FORMAT(F6.2)                                                       JRP00360
  WRITE(6,3)                                                            JRP00370
3   FORMAT('+','ENTER VERTICAL DIMENSION')                            JRP00380
  READ(5,2)XLONG                                                       JRP00390
  XLAT=XLAT-0.375                                                       JRP00400
  XLONG=XLONG-1.0                                                       JRP00410
  PHIR=(IDEG+(MIN+SEC/60.)/60.)*3.14159265/180.                      JRP00420
  GAMR=(IDEG1+(MIN1+SEC1/60.)/60.)*3.14159265/180.                  JRP00430
  YCP=XLAT/2.0                                                         JRP00440
  XCP1=XLONG/2.0                                                       JRP00450
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC JRP00460
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC JRP00470
  CALL TDS(TD)                                                         JRP00480
  DRPOS(1)=IDEG+(MIN+SEC/60.)/60.                                       JRP00490
  DRPOS(2)=IDEG1+(MIN1+SEC1/60.)/60.                                    JRP00500
  WRITE(6,10) IDEG,MIN,SEC, IDEG1,MIN1,SEC1                             JRP00510
10  FORMAT(' ','LATITUDE= ',I2,' ',I2,' ',I2,' ',F5.2,'LONGITUDE= ',I2
>,' ',I2,' ',I2,' ',F5.2)                                             JRP00520
  IF(A.GT.20.0)GOTO 45                                                 JRP00540
  DO 40 K=1,4,1                                                         JRP00550

```


DM(7)=3.0	JRP02760
DM(8)=54.0	JRP02770
CS(1)=50.47	JRP02780
CS(2)=34.44	JRP02790
CS(3)=11.98	JRP02800
CS(4)=40.51	JRP02810
CS(5)=50.47	JRP02820
CS(6)=33.44	JRP02830
CS(7)=45.61	JRP02840
CS(8)=47.20	JRP02850
RETURN	JRP02860
END	JRP02870
SUBROUTINE DATAY7	JRP02880
COMMON/CHAIND/DEL(2),A5,A6,AD(8),DM(8),CS(8)	JRP02890
DEL(1)=39.0E3	JRP02900
DEL(2)=54.0E3	JRP02910
A5=2.129260E4	JRP02920
A6=2.121045E4	JRP02930
AD(1)=42.0	JRP02940
AD(2)=76.0	JRP02950
AD(3)=34.0	JRP02960
AD(4)=77.0	JRP02970
AD(5)=42.0	JRP02980
AD(6)=76.0	JRP02990
AD(7)=39.0	JRP03000
AD(8)=87.0	JRP03010
DM(1)=42.0	JRP03020
DM(2)=49.0	JRP03030
DM(3)=03.0	JRP03040
DM(4)=54.0	JRP03050
DM(5)=42.0	JRP03060
DM(6)=49.0	JRP03070
DM(7)=51.0	JRP03080
DM(8)=29.0	JRP03090
CS(1)=50.47	JRP03100
CS(2)=34.44	JRP03110
CS(3)=45.96	JRP03120
CS(4)=46.76	JRP03130
CS(5)=50.47	JRP03140
CS(6)=34.44	JRP03150
CS(7)=07.46	JRP03160
CS(8)=12.14	JRP03170
RETURN	JRP03180
END	JRP03190
SUBROUTINE NEWDAT(I7,I,I2,J,J2)	JRP03200
COMMON/CHAIND/DEL(2),A5,A6,AD(8),DM(8),CS(8)	JRP03210
IF(I7-2)10,20,30	JRP03220
10 I=1	JRP03230
J=2	JRP03240
I2=1	JRP03250
J2=2	JRP03260
CALL DATAW	JRP03270
GO TO 40	JRP03280
20 I=2	JRP03290
J=3	JRP03300

APPENDIX B. Listing of TDPOS Program

FILE: TDPOS FORTRAN C OHIO UNIVERSITY AVIONICS ENGINEERING CENTER

```

SUBROUTINE TDPOS(TH,POS,DRPOS,IEPROR)                                TDP00010
DIMENSION IQSV(2),OSV(2),ANG(8),AD(8),OM(8),CS(8),POS(2),ZTWD(2),FTDP00020
:WM(2),DEL(2),TDR(2),DRD(2),DRM(2),TH(2),A(11),B(11),C(11),D(11),E(TDP00030
:11),CC(11),TM(2),BLEM(2),BEDEL(2),RADR(2),BETA(2),OMG(2),TWD(2),TDTDP00040
:PD(2),DRPOS(2)                                                    TDP00050
C -                                                                    TDP00060
DATA A1/24.0305/,A2/-0.40758/,A3/3.46776E-3/,B1/0.510483/,B2/-0.01TDP00070
:1402/,B3/0.001760/,R0/1.745329E-2/,RM/2.908882E-4/,RS/4.848137E-6/TDP00080
:,PI/3.141592/,A4/2.996912E2/                                      TDP00090
C -                                                                    TDP00100
COMMON/CHAIND/DEL,A5,A6,AD,OM,CS                                  TDP00110
C -                                                                    TDP00120
C - BEGIN TIME DIFFERENCE TO POSITION CONVERSION.                  TDP00130
C -                                                                    TDP00140
DO 1 I=1,2                                                         TDP00150
IDRD(I)=DRPOS(I)                                                  TDP00160
DRD(I)=IDRD(I)                                                    TDP00170
1 DRM(I)=(DRPOS(I)-DRD(I))*60.0                                    TDP00180
IEPROR=1                                                           TDP00190
A10=(A5*A5-A6*A6)/(A5*A5)                                         TDP00200
A14=1.0-A6/A5                                                     TDP00210
A50=(1.0+A14+A14*A14)                                             TDP00220
A51=(A50-1.0)                                                     TDP00230
A52=(A14*A14)/2.0                                                 TDP00240
A53=-A51/2.0                                                      TDP00250
A54=(A14*A14)/16.0                                               TDP00260
A55=(A14*A14)/8.0                                                TDP00270
A56=A14*A14                                                       TDP00280
A57=A56*1.25                                                      TDP00290
A58=A56/4.0                                                       TDP00300
DO 128 K=1,8                                                       TDP00310
IF(AD(K))124,126,126                                             TDP00320
124 ANG(K)=PD*AD(K)-RM*OM(K)+RS*CS(K)                             TDP00330
GO TO 128                                                         TDP00340
126 ANG(K)=PD*AD(K)+RM*OM(K)+RS*CS(K)                             TDP00350
128 CONTINUE                                                       TDP00360
A12=(ANG(1)-ANG(5)+ANG(2)-ANG(6))                                 TDP00370
A12=ABS(A12)                                                       TDP00380
IF(A12-0.00001)7,7,8                                             TDP00390
7 A11=-1.0                                                         TDP00400
GO TO 9                                                            TDP00410
8 A11=1.0                                                          TDP00420
C -                                                                    TDP00430
C - APPROXIMATE POSITIONS AND STATION COORDINATES.              TDP00440
C -                                                                    TDP00450
9 F(1)=ANG(1)                                                       TDP00460
F(2)=ANG(2)                                                       TDP00470
CC(1)=ANG(3)                                                       TDP00480
CC(2)=ANG(4)                                                       TDP00490
F(3)=SIN(E(1))                                                    TDP00500
F(4)=COS(E(1))                                                    TDP00510
F(5)=F(3)/F(4)                                                    TDP00520
F(8)=(F(5))*(1.0-A14)                                             TDP00530
A62=ATAN(E(8))                                                    TDP00540
F(6)=SIN(A62)                                                     TDP00550

```

```

      F(7)=COS(A62)
      CC(3)=SIN(CC(1))
      CC(4)=COS(CC(1))
      CC(5)=CC(3)/CC(4)
      CC(8)=(CC(5))*(1.0-A14)
      A62=ATAN(CC(8))
      CC(6)=SIN(A62)
      CC(7)=COS(A62)
      I=1
      GO TO 500
15  F(9)=A35
      F(10)=A46
      F(11)=A47
      DO 17 J=1,11
      A(J)=F(J)
17  B(J)=CC(J)
      F(1)=ANG(5)
      F(2)=ANG(6)
      CC(1)=ANG(7)
      CC(2)=ANG(8)
      E(3)=SIN(F(1))
      E(4)=COS(F(1))
      E(5)=E(3)/E(4)
      E(8)=(E(5))*(1.0-A14)
      A62=ATAN(E(8))
      F(6)=SIN(A62)
      F(7)=COS(A62)
      CC(3)=SIN(CC(1))
      CC(4)=COS(CC(1))
      CC(5)=CC(3)/CC(4)
      CC(8)=(CC(5))*(1.0-A14)
      A62=ATAN(CC(8))
      CC(6)=SIN(A62)
      CC(7)=COS(A62)
      I=2
      GO TO 500
19  F(9)=A35
      F(10)=A46
      F(11)=A47
      DO 21 J=1,11
      C(J)=F(J)
21  D(J)=CC(J)
      TM(1)=A(10)+A(11)
      TM(2)=C(10)+C(11)
      DO 45 M=1,2
      BETA(M)=TM(M)
      BDEF(M)=BETA(M)+DEF(M)
45  BLEF(M)=BETA(M)+BDEF(M)
      IOSV(1)=99999
      IOSV(2)=99999
      ITP=0
82  SDR=DRD(1)+DRM(1)+DRD(2)+DRM(2)
      IF(SDR) 83,84,83
93  DO 30 K=1,2
      IF(DRD(K)) 32,34,34

```

```

TDP00560
TDP00570
TDP00580
TDP00590
TDP00600
TDP00610
TDP00620
TDP00630
TDP00640
TDP00650
TDP00660
TDP00670
TDP00680
TDP00690
TDP00700
TDP00710
TDP00720
TDP00730
TDP00740
TDP00750
TDP00760
TDP00770
TDP00780
TDP00790
TDP00800
TDP00810
TDP00820
TDP00830
TDP00840
TDP00850
TDP00860
TDP00870
TDP00880
TDP00890
TDP00900
TDP00910
TDP00920
TDP00930
TDP00940
TDP00950
TDP00960
TDP00970
TDP00980
TDP00990
TDP01000
TDP01010
TDP01020
TDP01030
TDP01040
TDP01050
TDP01060
TDP01070
TDP01080
TDP01090
TDP01100

```

32	RADR(K)=RD*DRD(K)-RM*DRM(K)	TDP01110
	GO TO 30	TDP01120
34	RADR(K)=RD*DRD(K)+RM*DRM(K)	TDP01130
30	CONTINUE	TDP01140
	F(1)=RADP(1)	TDP01150
	F(2)=RADP(2)	TDP01160
	A2R=-1.0	TDP01170
84	F(3)=SIN(F(1))	TDP01180
	F(4)=COS(F(1))	TDP01190
	F(5)=F(3)/F(4)	TDP01200
	F(8)=(F(5))*(1.0-A14)	TDP01210
	A62=ATAN(F(8))	TDP01220
	F(6)=SIN(A62)	TDP01230
	F(7)=COS(A62)	TDP01240
	DO 86 J=1,8	TDP01250
86	CC(J)=D(J)	TDP01260
	I=3	TDP01270
	GO TO 500	TDP01280
90	C1=A35	TDP01290
	C2=A44	TDP01300
	C3=A45	TDP01310
	C101=A47	TDP01320
	DO 92 J=1,8	TDP01330
92	CC(J)=C(J)	TDP01340
	I=4	TDP01350
	GO TO 500	TDP01360
95	C4=A35	TDP01370
	C5=A44	TDP01380
	C6=A45	TDP01390
	C104=A47	TDP01400
	DO 50 J=1,8	TDP01410
50	CC(J)=R(J)	TDP01420
	I=5	TDP01430
	GO TO 500	TDP01440
55	C7=A35	TDP01450
	C8=A44	TDP01460
	C9=A45	TDP01470
	C107=A47	TDP01480
	IF(A11)52,99,53	TDP01490
53	C10=C7	TDP01500
	C11=C8	TDP01510
	C12=C9	TDP01520
	C110=C107	TDP01530
	DO 53 J=1,8	TDP01540
53	CC(J)=A(J)	TDP01550
	I=6	TDP01560
	GO TO 500	TDP01570
65	C7=A35	TDP01580
	C8=A44	TDP01590
	C9=A45	TDP01600
	C107=A47	TDP01610
	C13=TH(2)-C(10)-C(11)-C101+C104-DEL(2)	TDP01620
	C17=C13*A4	TDP01630
	C18=TH(1)-A(10)-A(11)-C110+C107-DEL(1)	TDP01640
	C22=C18*A4	TDP01650

```

      DO 4840 M=1,2
      W=DMG(M)/RD
      IWD(M)=W
      FWD=IWD(M)
      DWD=W-FWD
      EWM=DWD*60.0
      FWM(M)=ABS(EWM)
      IF(FWM(M)-59.9995)4840,4810,4810
4810 FWM(M)=0.0
      IF(IWD(M))4820,4830,4830
4820 IWD(M)=IWD(M)-1
      GO TO 4840
4830 IWD(M)=IWD(M)+1
4840 CONTINUE
      GO TO 900
C -
C - CALCULATION OF INVERSE VARIABLES.
C -
500 A59=-CC(2)
      A60=-F(2)
      C35=A59-A60
      C36=ABS(C35)
      IF(C36-0.1)501,502,502
502 A16=2.0*01-C36
      GO TO 505
501 A16=C36
505 IF(A16)506,507,506
507 A16=0.00000005
506 A17=SIGN(A16)
      A18=COS(A16)
      A19=F(6)*CC(6)
      A20=F(7)*CC(7)
      A21=A19+A20*A18
      A22=((A17*CC(7))**2+(CC(6)*F(7)-F(6)*CC(7)*A18)**2)**0.5
      A23=(A20*A17)/A22
      A24=1.0-A23*A23
      A25=ARCTN(A22)
      A26=A25*A25
      A27=1.0/A22
      A28=A21/A22
      A29=A24*A24
      A30=(A50*A25)+A19*(A51*A22-A52*A26*A27)
      A31=A24*(A53*A25+A53*A22*A21+A52*A26*A28)
      A32=A19*A19*(-A52*A21*A22)
      A33=A29*(A54*A25+A54*A21*A22-A52*A26*A28-A55*A22*(A21**3))
      A34=A19*A24*(A52*A26*A27+A52*A22*A21*A21)
      A35=(A30+A31+A32+A33+A34)*A6*A4
      A36=(A51*A25)+A19*(-A52*A22-A14*A14*A26*A27)
      A37=A24*(-A57*A25+A58*A22*A21+A14*A14*A26*A28)
      A38=(A36+A37)*A23+A16
      A39=SIGN(A38)
      A40=COS(A38)
      A41=(CC(6)*F(7)-A40*F(6)*CC(7))/(A39*CC(7))
      IF(A41)510,509,510
509 A41=0.00000005

```

```

TOP02210
TOP02220
TOP02230
TOP02240
TOP02250
TOP02260
TOP02270
TOP02280
TOP02290
TOP02300
TOP02310
TOP02320
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TOP02340
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TOP02560
TOP02570
TOP02580
TOP02590
TOP02600
TOP02610
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TOP02630
TOP02640
TOP02650
TOP02660
TOP02670
TOP02680
TOP02690
TOP02700
TOP02710
TOP02720
TOP02730
TOP02740
TOP02750

```

```

C23=C1-C17
C24=C4
C25=C7+C22
C26=C10
C27=(C2-C5)*(C25-C26)+(C23-C24)*(C11-C8))
C29=(C2-C5)*(C12-C9)+(C3-C6)*(C8-C11))
C30=C27/C29
C28=(C23-C24+C30*(C3-C6))/(C5-C2)
GO TO 130
52 C13=TH(2)-C(10)-C(11)-C101+C104-DFL(2)
C17=C13*A4
C18=TH(1)-A(10)-A(11)-C107+C104-DFL(1)
C22=C18*A4
C23=C1-C17
C24=C4
C25=C7-C22
C27=(C2*(C25-C24)+C23*(C5-C8)+C8*C24-C5*C25)
C29=(C2*(C6-C9)+C3*(C8-C5)+C5*C9-C8*C6)
C30=C27/C29
C28=(C23-C24+C30*(C3-C6))/(C5-C2)
130 C31=(A5*A4*(1.0-A10))/(1.0-A10*F(3)*F(3))*.5
C32=(A5*A4)/(1.0-A10*F(3)*F(3))*.5
C33=(C30/C31)
C34=(-C28/(C32*F(4)))
F(1)=F(1)+C33
E(2)=F(2)+C34
IF(A28)132,99,134
132 A28=1.0
GO TO 84
C -
C - CONVERSION DONE, RETURN TO DISTANCE-BEARING ROUTINE.
C -
900 IF(IQSV(1).NE.IWD(1))GO TO 7713
IF(IQSV(2).NE.IWD(2))GO TO 7713
IF(ABS(QSV(1)-FWM(1)).GT.0.1)GO TO 7713
IF(ABS(QSV(2)-FWM(2)).GT.0.1)GO TO 7713
IDR(I)=IDR(I)*10
DO 839 I=1,2
ZIWD(I)=IWD(I)
939 POS(I)=ZIWD(I)+FWM(I)/60.0
RETURN
C -
C - CONTINUE ITERATIONS.
C -
7713 DO 7712 M=1,2
DRD(M)=0.0
DRM(M)=0.0
QSV(M)=FWM(M)
7712 IQSV(M)=IWD(M)
ITER=ITER+1
IF(ITER.LT.100)GO TO 82
IFRDR=-1
RETURN
134 DMG(1)=F(1)
DMG(2)=F(2)

```

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TDP01660
TDP01670
TDP01680
TDP01690
TDP01700
TDP01710
TDP01720
TDP01730
TDP01740
TDP01750
TDP01760
TDP01770
TDP01780
TDP01790
TDP01800
TDP01810
TDP01820
TDP01830
TDP01840
TDP01850
TDP01860
TDP01870
TDP01880
TDP01890
TDP01900
TDP01910
TDP01920
TDP01930
TDP01940
TDP01950
TDP01960
TDP01970
TDP01980
TDP01990
TDP02000
TDP02010
TDP02020
TDP02030
TDP02040
TDP02050
TDP02060
TDP02070
TDP02080
TDP02090
TDP02100
TDP02110
TDP02120
TDP02130
TDP02140
TDP02150
TDP02160
TDP02170
TDP02180
TDP02190
TDP02200

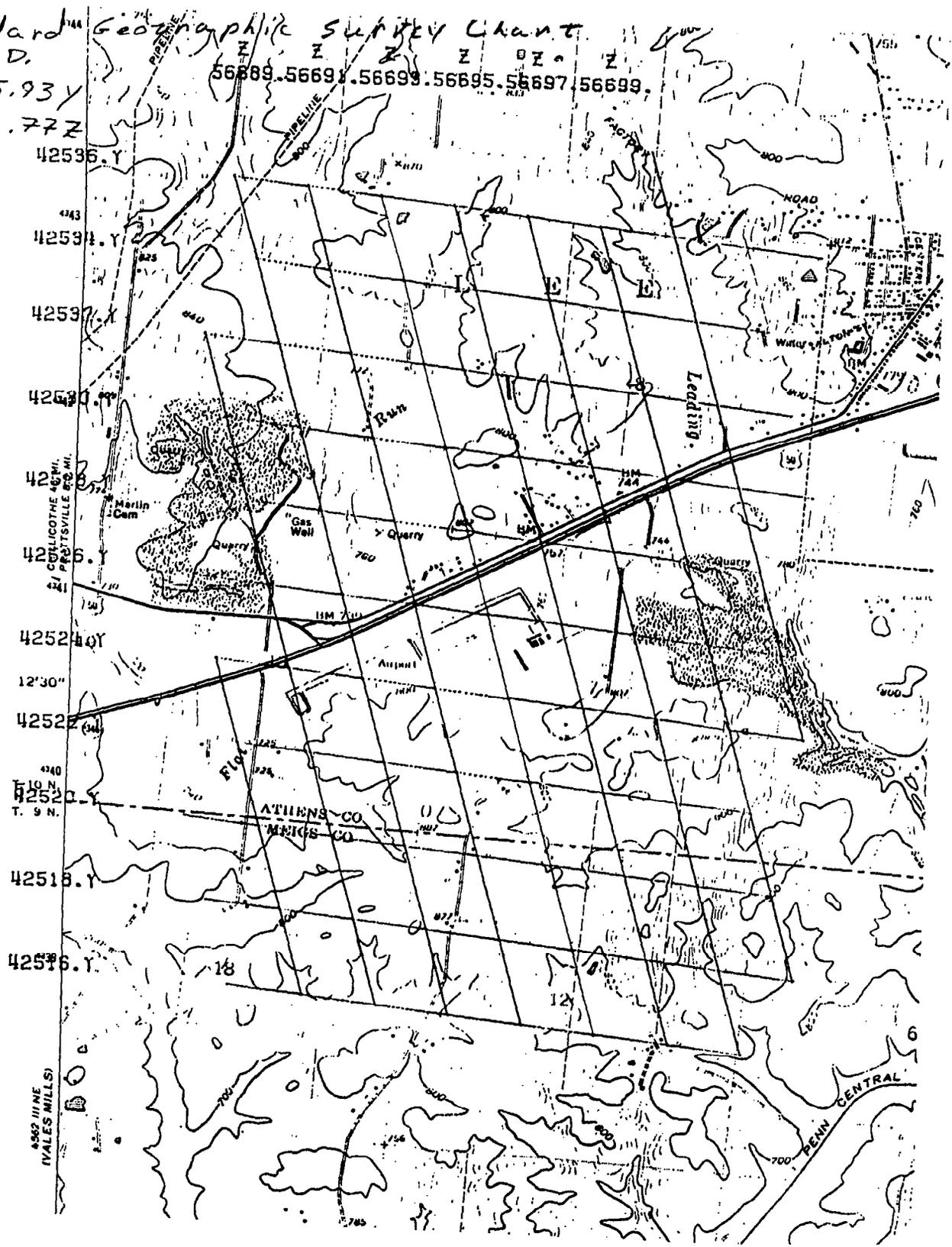
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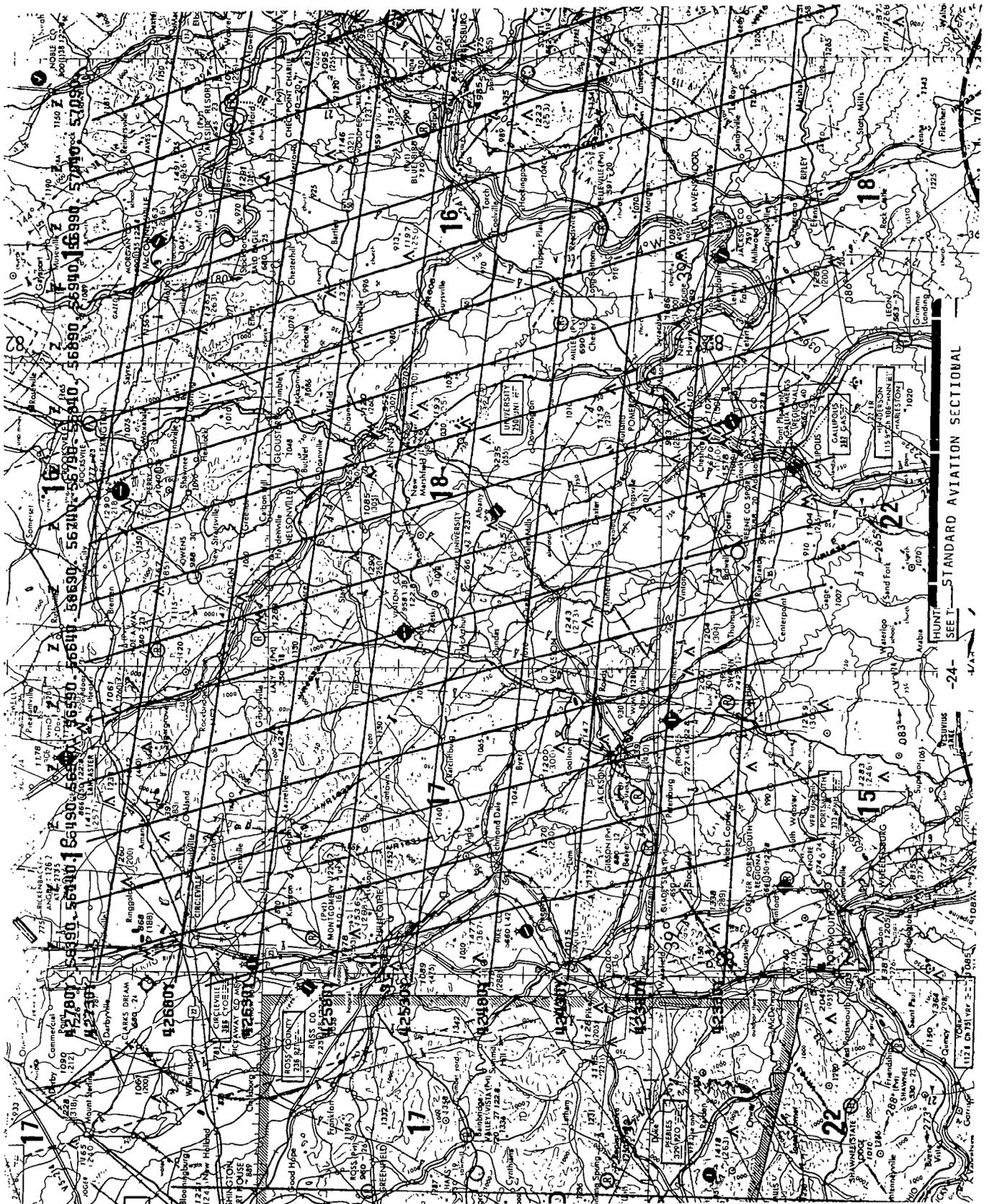
510	A42=1.0/A41	TDP02760
	A43=ATAN(A42)	TDP02770
	IF(C35)515,514,514	TDP02780
514	IF(C35-P1)511,512,512	TDP02790
511	IF(A41)520,521,521	TDP02800
520	A43=P1+A43	TDP02810
	GO TO 521	TDP02820
512	IF(A41)517,518,518	TDP02830
515	IF(C35+P1)511,511,516	TDP02840
516	IF(A41)517,518,518	TDP02850
517	A43=P1-A43	TDP02860
	GO TO 521	TDP02870
518	A43=2.0*P1-A43	TDP02880
521	A43=A43+P1	TDP02890
	A43=A43-2.0*P1	TDP02900
	IF(A43)522,523,523	TDP02910
522	A43=A43+2.0*P1	TDP02920
523	A44=SIN(A43)	TDP02930
	A45=COS(A43)	TDP02940
	A46=A35/1609.344	TDP02950
	IF(A46-100.0)525,526,526	TDP02960
525	A47=P1/A46+P2+P3*A46	TDP02970
	GO TO 527	TDP02980
526	A47=A1/A46+A2+A3*A46	TDP02990
527	A46=A35/A4	TDP03000
	GO TO(15,19,90,95,55,65),I	TDP03010
99	RETURN	TDP03020
	END	TDP03030

APPENDIX C. Sample Charts with Lines of Position

Standard Geographic Survey Chart
C. P. T. D.
42525.93 Y
56692.77 Z

56689.56691.56693.56695.56697.56699.





TECHNICAL MEMORANDUM OU NASA 79

AUTOMATIC GAIN CONTROL

An automatic gain control has been designed and fabricated to operate with the Loran-C prototype receiver and data collection system currently in use at Ohio University.

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I. INTRODUCTION

The NASA Tri-University program at Ohio University is currently involved in the development of a low-cost Loran-C receiver for use in general aviation aircraft. An automatic gain control (AGC) has been designed and built to operate with the prototype Loran-C receiver.

Since there are such extreme distances between Loran stations, the signal strengths coming into the user are at different magnitudes. It is advantageous to have the signal magnitudes equal; therefore, the automatic gain control was designed for the front end of the prototype Loran-C receiver.

II. CIRCUIT DESCRIPTION

The automatic gain control is a three-transistor circuit (see Figure 1) which requires a constant D.C. voltage of 8 volts. Tests conclude that this value may be in the range of 4 to 12 V without change in circuit performance. Transistors Q_1 and Q_2 are cascaded to pass and amplify the input signal. The gain of Q_1 and Q_2 is controlled by Q_3 which itself is controlled by an external AGC voltage between 0 and 8 volts D.C. The integrated circuit used is an RCA CA3028A, an 8-pin chip, which is a differential cascode amplifier designed for use in communications operating at frequencies from D.C. to 120 MHz. The integrated circuit has been balanced for AGC capabilities, and has a wide operating current range. The maximum input current at pins 1 and 5 is 0.1 mA. The absolute maximum dissipation at $T_a \leq 85^\circ \text{C}$ is 450 mW. At $T_a > 85^\circ \text{C}$ the integrated circuit is derated linearly 5 mW/ $^\circ \text{C}$. The ambient temperature for operation is -55°C to $+125^\circ \text{C}$ and -65°C to $+150^\circ \text{C}$ for storage.

III. TEST RESULTS

1. Gain Vs. Frequency and Phase Angle Vs. Frequency (Figure 2)

The frequency response and phase angle is measured with the input signal voltage held constant at 50 mV, and is an average of all AGC voltages from 1 V to 8 V. The band width of the automatic gain control is 20 KHz to 2 MHz, with a standard deviation of no greater than ± 0.4 dB. The phase angle increases linearly at frequencies between 70 KHz to 120 KHz, from 0° to $+21.6^\circ$ respectively.

2. Gain Vs. AGC Voltage (Figure 3)

This test was performed at a constant frequency of 105.4 KHz and a constant input signal voltage of 50 mV. The gain is approximately -26 dB from 0 to +2.5 volts, between 1 and 2.5 volts the gain increases rapidly from -22 dB to +2.5 dB, between 3 and 8 volts the gain increases from 2.5 dB to 25 dB. Distortion and gain compression occurs at 8.4 volts AGC and loss of gain occurs at AGC voltages greater than 12 volts.

3. Gain Vs. Signal Voltage (Figure 4)

This test was performed at a constant frequency of 100 KHz and is an average of AGC voltages from 3 to 8 volts. The operating recommended input voltages are between 5mV and 75 mV. In this range there was a constant gain with a standard deviation of only ± 0.109 dB.

4. Power Dissipation and Circuit Resistance

This test was performed at a frequency of 100 KHz with an input signal voltage of 50 mV. The circuit draws 50 mA constant current. The D.C. power dissipation was 59 mW (Max. $P_{D,C}$ dissipation 450 mW). A.C. current at pins 1 and 5 is approximately $61.21 \mu A$ at 100 KHz. The A.C. power dissipation is approximately 3.035×10^{-6} watts with a power factor of .9 leading calculated error for A.C. power is 4.1%.

Circuit Resistance

$$\text{Input Resistance } R_i' = 140 \Omega$$

$$\text{Output Resistance } R_o' = 740 \Omega$$

IV. SUMMARY

The automatic gain control was designed specifically to operate with the prototype Loran-C receiver and data collection system. The use of the automatic gain control is intended to eliminate error which occurs when signals are received at different magnitudes.

V. ACKNOWLEDGEMENTS

The design and construction of the automatic gain control was supported by the NASA Tri-University program and is part of the development of a low-cost Loran-C navigation receiver for general aviation aircraft. The author would like to thank Mr. Ralph Burhans of the Ohio University Avionics Engineering Center who designed the automatic gain control.

VI. BIBLIOGRAPHY

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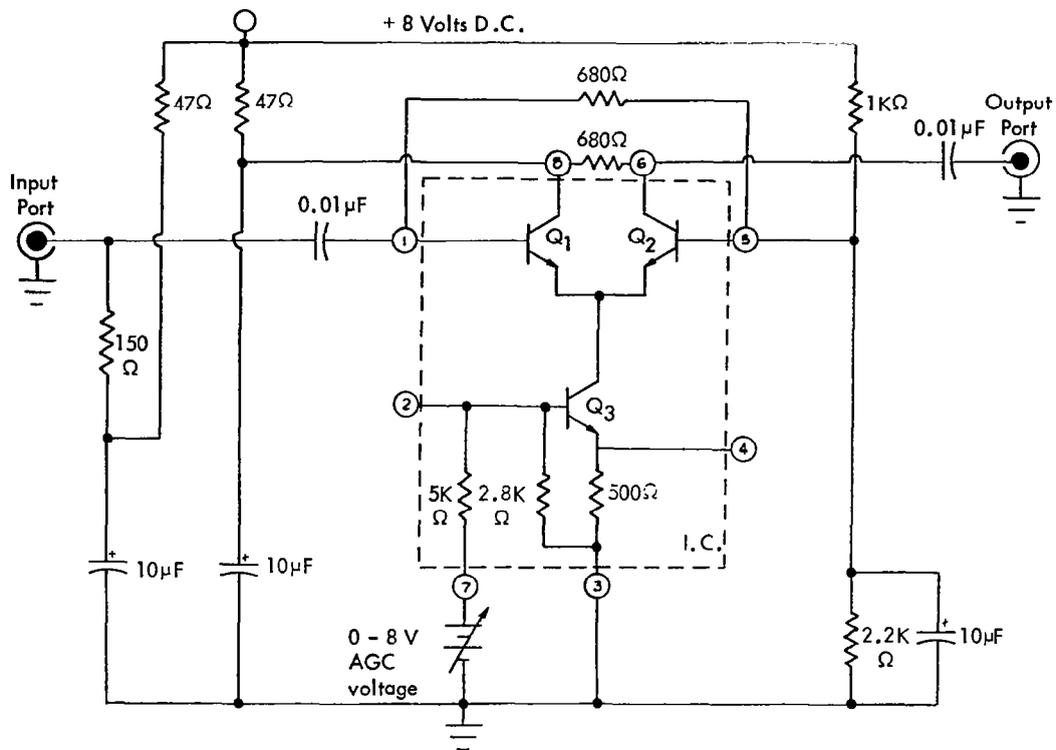


Figure 1. Automatic Gain Control Circuit.

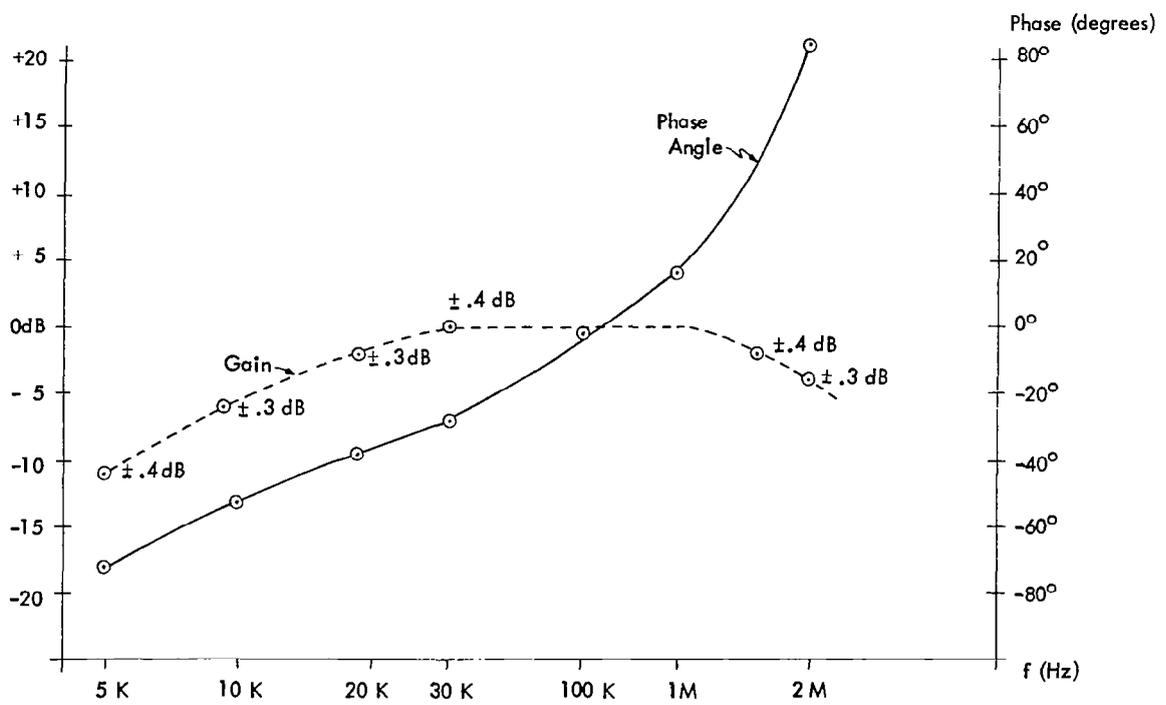


Figure 2. Phase Angle Vs. Frequency.

f = 100 KHz
Input Magnitude 50mV

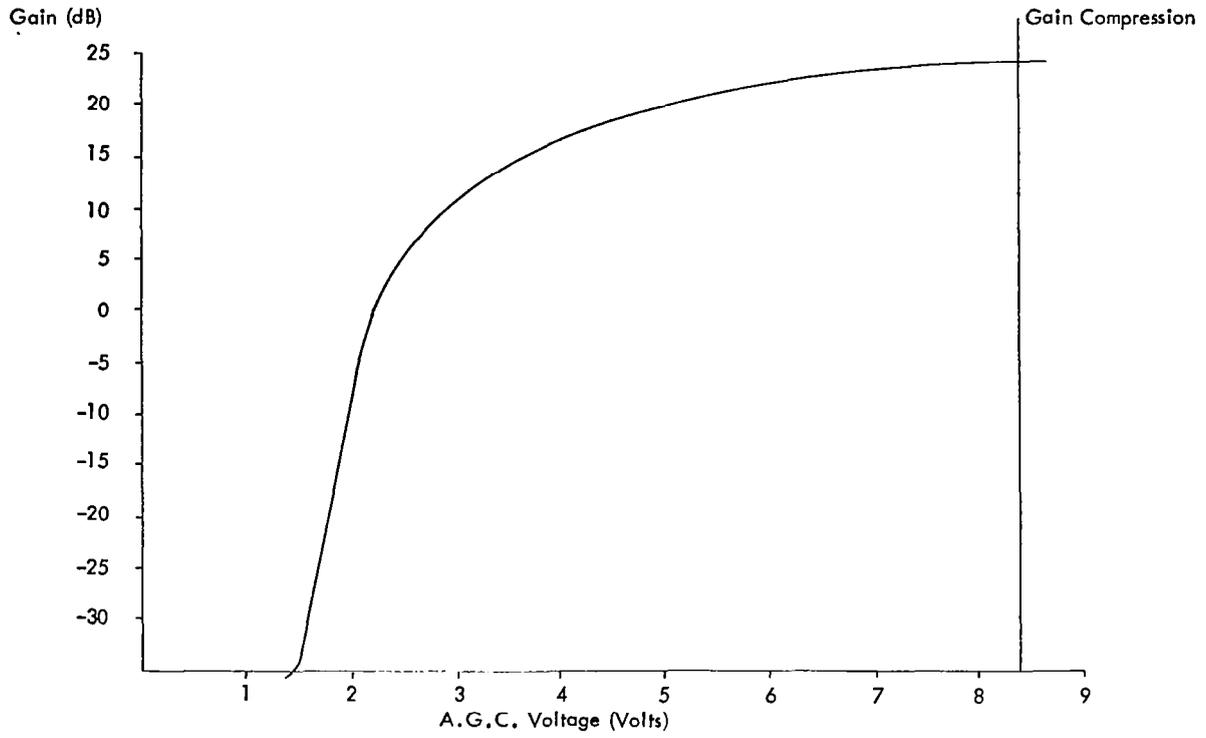


Figure 3. Gain Vs. A.G.C. Voltage.

Gain Vs. Signal Magnitude
f = 100 KHz

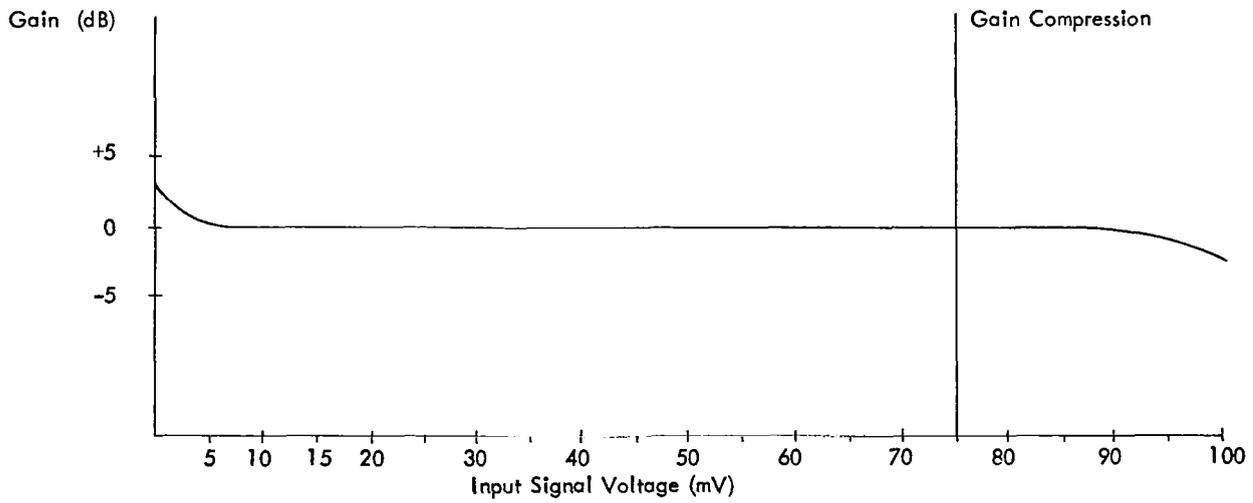


Figure 4. Gain Vs. Signal Voltage.

TECHNICAL MEMORANDUM OU NASA 80

A LORAN-C PROTOTYPE NAVIGATION RECEIVER
FOR GENERAL AVIATION

The design, fabrication and evaluation of a prototype Loran-C receiver is described. Hardware is complete, and microcomputer programming continues, for addition of area-navigation capability. The receiver is an envelope-processor, offering simplicity of RF processor circuitry.

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I. INTRODUCTION

The Avionics Engineering Center, Ohio University Department of Electrical Engineering, has pursued the techniques required for Loran-C navigation with application to the general-aviation pilot. The goal has been to produce prototype equipment for flight evaluation which will provide enroute navigation in both latitude-longitude and rho-theta coordinates and to evaluate the non-precision approach capabilities of such equipment.

For this prototype project, single-chain, master-dependent operation was chosen as a demonstration mode, with three stations tracked. The prototype hardware design will, however, permit cross-chain, master-independent navigation. The number of stations tracked simultaneously can be expanded. These extended operating modes are implemented through programming utilizing existing shared tracking-loop hardware as described below.

The prototype Loran-C receiver has been flight-tested using a variety of flight paths, with and without simultaneous ground radar position data collection. Results are presented later in this paper; further flight evaluation is planned, and will be reported separately.

The following sections describe major receiver elements, drawing upon the work and publications of project team members who contributed to the design.

II. RECEIVER OVERVIEW

As configured for laboratory and flight evaluation (Figure 1), the prototype Loran-C receiver utilizes an aircraft ADF sense antenna or similar unit, connected directly to the wide-band preamplifier/coupler. Signal levels for the linear RF processor are stabilized by a commutated, sampled AGC element, under control of the receiver computer.

The RF unit performs analog signal processing and conversion to TTL-compatible output pulses corresponding to Loran-C envelope events. For the prototype receiver, a commercially-available microcomputer is utilized for both sensor and navigation processing, plus AGC control. Computer control and data recording for experimentation are provided by a hand-held ASCII terminal and either analog or digital cassette units.

Pilot control of receiver functions is effected through the panel-mounted keyboard and video display unit, supported by a video processor board with independent memory. The receiver computer is, in this prototype implementation, supported by a mathematical function processor chip, aiding in the coordinate conversion from Loran-C to geodetic coordinates, and for rho-theta conversions.

III. ANTENNA PREAMPLIFIER/COUPLER

The Loran-C prototype utilizes the wide-band preamplifier of the type reported by Burhans [1, 2, 3] for connection to either a 1-meter (or larger) whip antenna for laboratory tests or to the existing ADF sense antenna aboard the test aircraft. This preamplifier, illustrated in Figure 2, provides -4.9 dB voltage gain at 100 kHz, matching a High-Z antenna to a 1000 ohm receiver input impedance, and a dynamic range from 0.2 to 10,000 microvolts rms at the input terminal. Preamplifier 3 db points occur at 10 Hz and 8 MHz.

The preamplifier schematic is shown as Figure 3. Input surge protection is provided by the NE-2 bulb at the input terminal. The low-noise JFET drives an open-collector output stage, the load resistor for which is contained in the receiver RF module. Both DC power and signal use the signal coaxial cable connecting the preamplifier to the receiver RF section, eliminating power-supply ground-loop problems.

IV. LORAN-C RF PROCESSOR

The Loran-C receiver RF processor is based on an auto-correlation envelope detector. The unit is driven by the low-impedance output of the broadband, unity-gain antenna preamplifier. See Figures 4, 5 and 6.

The input circuit is a broad-tuned transformer with a 40kHz bandwidth, centered at 100kHz. The output of this transformer is placed across a 1K ohm potentiometer, the wiper of which controls the amount of signal provided to the trap circuitry. Note that this voltage-divider circuit has created a passive RF gain control, to which the operator has access in the prototype design.

To improve signal-to-noise ratio (with respect to interfering frequencies) of the Loran-C signal, it is desirable to eliminate strong signals close to the 100 kHz region before the RF is actively amplified. This is accomplished by passing the RF through a pair of notch filters. These narrowband filters are centered at 88 kHz and 119 kHz, to eliminate the 88 kHz, 116 kHz, and 122 kHz interfering frequencies affecting the 99600 U.S. Northeast Chain. These interfering frequencies are listed in the May 1980 edition of the Loran-C User Handbook by the U.S. Coast Guard [4].

Current work is underway to investigate distortion products from multiple RF signals and harmonic mixing or multiplying to produce new frequencies that interfere with Loran-C. Research results and documentation of this work will be available from the Avionics Engineering Center through the NASA Joint University Program.

Once the interfering frequencies are minimized, the RF signal is amplified by a tuned RF amplifier. This TL072 operational

amplifier circuit offers +30 dB gain with a 30 kHz bandwidth, centered at 100 kHz. The RF signal flow now branches into two separate paths, to be manipulated separately to create the RF signals required for the LM2111 FM Detector and Limiter. One path drives a T-notch filter tuned to 100 kHz which delays the RF signal and adds the delayed reproduction to the actual incoming RF (delay-and-add). The delayed-and-added signal is then amplified by a broadband, +30 dB gain TL072. This signal path is terminated at one of the RF inputs to the balanced demodulator of the LM2111. The second path drives the RF limiter of the LM2111 (the limiter has +60 dB gain), which in turn provides the signal for the second RF input of the balanced demodulator and the carrier zero-crossing detector.

The LM2111 IC provides a double-balanced active multiplier used as an envelope detector. The demodulated signal is fed to a lowpass RC filter (20 kHz bandwidth), creating the Loran-C envelope, from which the digital output is derived. An envelope level detector produces a digital pulse at the zero crossing of the rising edge of the Loran-C envelope. This pulse, correlated with the zero crossings of the RF carrier (from the output of the LM2111 limiter) produces the digital pulses to be used for signal processing. These pulses are stretched to 70 μ sec. to permit the tracking loop search routines to operate efficiently.

V. TRACKING LOOP HARDWARE

The Loran-C prototype receiver achieves time-difference measurement by use of a software-controlled, shared, digital loop. The block diagram for this loop circuit is shown in Figure 7, and its schematic in Figure 8. A 1 MHz clock drives the 6-digit BCD free-running counter portion of the MOSTEK 50395 integrated circuit, providing the receiver time base. The 6-digit comparator produces an EQ pulse each time the counter and the 6-digit register are identical.

In operation, the microcomputer loads the register with the count corresponding to the desired sample time for loop operation, while the counter continues to run. Equality of counter and register produces an EQ pulse, which is latched as an interrupt request (IRQ) for the microcomputer. At the time the EQ pulse is received, the Loran-C digital envelope signal is also latched, and its value made available to the microcomputer. The microcomputer may then reload the register for the next sample point, a process which has been measured to require 450 μ sec. The loop, therefore, is able to detect each envelope pulse, at the 1 msec. Loran-C interval, with sufficient guard time to insure correct operation.

The schematic shows interconnection between the tracking loop and the Super-Jolt (TM) microcomputer, which is used in the prototype receiver for evaluation. Pinouts are detailed in Figure 9. This 8-bit microcomputer is based upon the MOS Technology 6502 CPU chip, running at a 1 MHz clock rate. In the prototype receiver, the computer and loop clocks are obtained from the same TCXO for convenience, but computer software is entirely asynchronous, interrupt-driven code.

The digital loop circuit board is shown in Figure 10. The MOS Technology 50395 is visible as the 40-pin chip, supported by a 7474 latch for IRQ and Loran-C input latching, and one monostable multivibrator, 74123, to stretch the Loran-C digital RF processor outputs to 70 μ sec. for loop use. The remaining circuitry provides level shift services, to interface the MOS loop chip to TTL input/output lines for the microcomputer.

The entire loop circuit is operated by one 6520 PIA interface, which is an integral part of the Super-Jolt microcomputer.

VI. TRACKING LOOP PROGRAMMING

Initially, tracking loop software has been developed to demonstrate correct hardware operation and to provide a basis from which coordinate-conversion and area-navigation routines could be developed. This sensor processor software consists of signal acquisition, tracking and time-difference generation segments, operating on a single Loran-C chain. In the current implementation, three stations are tracked, one of which must be the master station.

Loop routines are initiated at receiver start-up, by user choice of Loran-C chain. This selection, made by entering the group repetition interval (GRI), causes the loop routine to add the GRI, in microseconds, to the loop register upon receipt of each loop interrupt request (IRQ). The result is a series of interrupts, at the GRI rate, with samples of Loran-C input data occurring with each interrupt. Loop arithmetic is continuous; that is, the counter is allowed to overflow at 10^6 counts, with no resulting effect on sample rate.

Each IRQ causes loop software to read the state of the Loran-C latch and to clear the Loran-C and IRQ latches. While in this acquisition mode, the goal of the loop routines is to find correlated signals at the Loran-C latch, compared with the GRI samples. If no occurrence of five contiguous Loran-C ones in 32 GRI frames is found, the acquisition segment modifies the sample time by adding 6,500 μ sec. to the register. This addition effectively delays the sample comb by 6,500 μ sec., and the test for Loran-C signals is repeated. After an unsuccessful test at the 6,500 μ sec. increment, the test is repeated for 36 mini-increments of 33 μ sec. each.

With each Loran-C pulse stretched to 70 μ sec., acquisition is generally accomplished in less than ten seconds. Once one Loran-C pulse is found, acquisition code passes control to station-track code, which immediately subtracts 2,000 μ sec. from the original register contents and repeats the acquisition test. If no pulse is found, the register is increased by 1,000 μ sec., and the test repeated. If a pulse is found, 2,000 μ sec. is subtracted again. In this manner, the first pulse of each Loran-C station is acquired.

Fine tracking begins at this point, with the station-track routine subtracting one microsecond when the Loran-C data is high, and

adding one microsecond when the Loran-C data is low. A loop filter is inserted at this point, in the form of an up-down software counter, to provide for optimum loop characteristics. Filter parameters are taken from previous theoretical [5] and experimental [6] work, and were chosen as a 5-bit register. When this register overflows, one microsecond is added to the loop register. Upon filter register underflow, one microsecond is subtracted. The result is a low-pass loop filter, with time constant of 4 GRI time periods. Using the first-pulse position in the loop register, determined by the search/track process just described, the station-track segment then generates eight sample pulses, by 1,000 μ sec. increments of the loop register, spaced one millisecond apart, and permits correction of the loop register value at each of the eight pulses.

After successful lock to the station, the loop register is incremented by 9035 μ sec., and the master 9th pulse is sought by the acquisition test. If found, the current station is labeled as the master, for use by background routines in computing time differences. The register content, representing the time of occurrence of the station first-pulse, is stored for retrieval at the next occurrence of the station's signal.

The loop software then generates a search pulse immediately after the last pulse for the current station, and the search/track process is repeated. The third station is located in the same manner.

In addition to the basic pulse-tracking function, the loop routines also produce a signal-quality number, useful in generating user warnings and assessing receiver operation. A software counter is incremented by one, for each station, when the loop routines must subtract one microsecond to retain lock. This counter is then cleared by background routines after display. In the current implementation, the counter is active for ten GRIs, resulting in a total pulse count opportunity of 80. In ideal conditions, with no noise present on the Loran-C input, the counter should reach one-half the total pulse count, since alternate additions and subtractions of one microsecond would be required to retain lock on each of the station pulses. Significant deviations from this value indicate the potential for loss of lock, and may be used to trigger re-acquisition of the station.

The background routines, which operate with IRQ enabled, execute when the signal-processing software just described is completed for each Loran-C pulse. A BCD buffer for each Loran-C station contains the loop register value generated in the previous GRI; these values are averaged over ten GRI periods, and the slave values subtracted from the master after averaging. The results are displayed as the time differences. The signal quality numbers are displayed also. Time difference data is placed in buffers for use by the latitude-longitude conversion routines.

The initial implementation of tracking loop programs has met the desired objective. The receiver logic has been demonstrated, and

loop parameters measured. It has been determined that the single microprocessor receiver will be capable of five-station tracking plus coordinate conversion, and that ample guard time exists between Loran-C envelope pulses for signal processing to take place, with the microcomputer operating at 1 MHz.

A counter/comparator IC offering faster digit-strobe operation would be a definite aid, as the scan oscillator on this IC is the limiting factor in register loading by the microcomputer.

The software-controlled tracking loop implementation has demonstrated some interesting by-products, in that the loop has applications in time synchronization and navigation audio processing not contemplated at its inception. Use of the loop in IRIG-B time synchronization, for example, has been accomplished with complete success. [7]

VII. VIDEO OUTPUT

A prototype video interface [8], designed specifically for large-character output for cockpit use, has been used throughout the receiver development and evaluation program. Figure 11 shows this video circuit board. With the forthcoming addition of rho-theta area-navigation software, this video interface will be exchanged for a smaller circuit board, able to display both character and graphics data.

Two-page output permits display of Loran-C time-difference data, signal quality and housekeeping data on one video page, and the latitude-longitude and range-bearing waypoint data on the other. With the graphics interface available, CDI information will be displayed on both pages, driven by the bearing-distance coordinate conversion routines.

Figure 12 shows the receiver package, with video monitor and keyboard installed. The Loran-C RF processor will be enclosed under the chassis for isolation from the digital circuitry and the video monitor oscillator, and the digital circuit boards will surround the monitor chassis. The package is standard general-aviation width, for mounting in the vertical stack. The power transformer visible at the rear of the unit is installed for bench testing only, and is not part of the final prototype, which will operate on 14VDC.

VIII. LABORATORY AND FLIGHT EVALUATION

Receiver tests run with a Loran-C simulator have consistently provided receiver time differences within ± 1 μ sec. of simulator outputs. These tests have also defined the need for receiver AGC applied station-by-station, due to TD offsets observed for variations in relative signal strength among stations. This AGC circuitry is currently under test.

Flight evaluations, made without AGC circuitry at Ohio University Airport, Athens, Ohio on March 9, 1981 are illustrated in Figures 13 and 14. These graphs are plots of receiver latitude/longitude outputs, converted to range and bearing from a waypoint.

For Figure 13, the waypoint is the calculated latitude and longitude of the runway center point. The flight path begins at point (1), on takeoff roll over the waypoint. The path proceeds on climb-out, heading 240° and through pattern turns at 800 feet AGL to crosswind and downwind legs. Downwind is extended to seven miles northeast of the airport, where the aircraft is turned inbound, across the UNI non-directional beacon, 5.3 nautical miles from threshold. A normal low approach is then executed, heading 243, flying visually along the runway centerline.

Following the low approach, a tight turn is made to a close downwind leg, followed by an outbound segment (2) approximately 30° south of centerline. A perpendicular cut across the UNI beacon (3) is then executed, followed by a turn (4) back to the beacon, and a left 270° turn to the inbound approach course. A second low approach along runway centerline is then executed, followed by landing and taxi operations.

The data presented is averaged by the receiver over a ten-GRI time period; approximately one second on the 99600 chain. Positioning repeatability over the UNI NDB and along the approach track are observed to be excellent. Long-term variations along the approach course tend to be well-correlated, with a peak variation of less than 600 feet. Note, however, the offset to the north, resulting in a track parallel to the desired runway centerline track, of approximately one-half mile. This offset has been determined using the laboratory simulator to be due to signal-strength characteristics among Loran-C stations in the local area.

Figure 14 shows Loran-C data, with one-second TD averaging and subsequent latitude/longitude conversion, presented as distance and bearing from the runway. For this flight, a receiver waypoint was determined by placing the aircraft stationary at the runway center point, and entering the resulting receiver latitude and longitude value as the waypoint. The flight then consists of a takeoff and climbout to 1000 feet AGL, on runway heading. Variations noted on this plot are a maximum of 0.4 nmi south of course, and 0.3 nmi to the north.

It should be noted that these flight evaluations were local, short flights to assess basic receiver operation and raw data stability. Current plans call for documented flights, including ground radar tracking for position reference, as soon as AGC circuitry is fully tested.

IX. CURRENT WORK IN PROGRESS

Tracking loop software changes are contemplated for five-station tracking with master independence. Decoded warning messages will be provided when the master 9th-pulse blink code is available. All valid time differences will be made available to the coordinate-conversion and area-navigation software, so that composite position fixes will be possible.

Initial flight evaluations have shown encouraging results, especially with regard to repeatability. Absolute accuracy in the first field tests suffered due to variations in signal strength among stations. A computer-controlled AGC, acting on each Loran-C envelope pulse and commutated among active stations, has been designed and is under test as of this writing. Initial results show marked improvement, with receiver bias reduced over 75% from operation without AGC, on the 9960 chain in southeastern Ohio.

The latitude/longitude and range/bearing coordinate conversion circuitry and software have been used routinely in receiver evaluation; the documentation for this portion of the receiver will appear [9] as a M.S. thesis in the near future.

Additional flight evaluations are planned, using ground-based radar for position reference data. Techniques and procedures for differential Loran-C are also under study, to determine whether receiver cost may be minimized by permitting a differential setting periodically during a flight, or prior to an approach.

X. ACKNOWLEDGEMENTS

The prototype Loran-C receiver is being developed under Grant NGR-36-009-017, supported by NASA Langley Research Center. Ralph W. Burhans, Project Engineer, developed receiver antenna preamplifier and RF processor units, with support from student intern James Roman. Tracking loop software development and keyboard interface were supported by intern Stan Novacki. M. S. Candidate Joe Fischer contributed the time-difference to latitude-longitude conversion hardware and software, and intern Steve Yost developed power supply and commutated AGC circuitry.

Personnel are members of the NASA Joint University Program in Air Transportation Systems at Ohio University; the program is carried out in cooperation with similar teams operating at MIT and Princeton University. [10]

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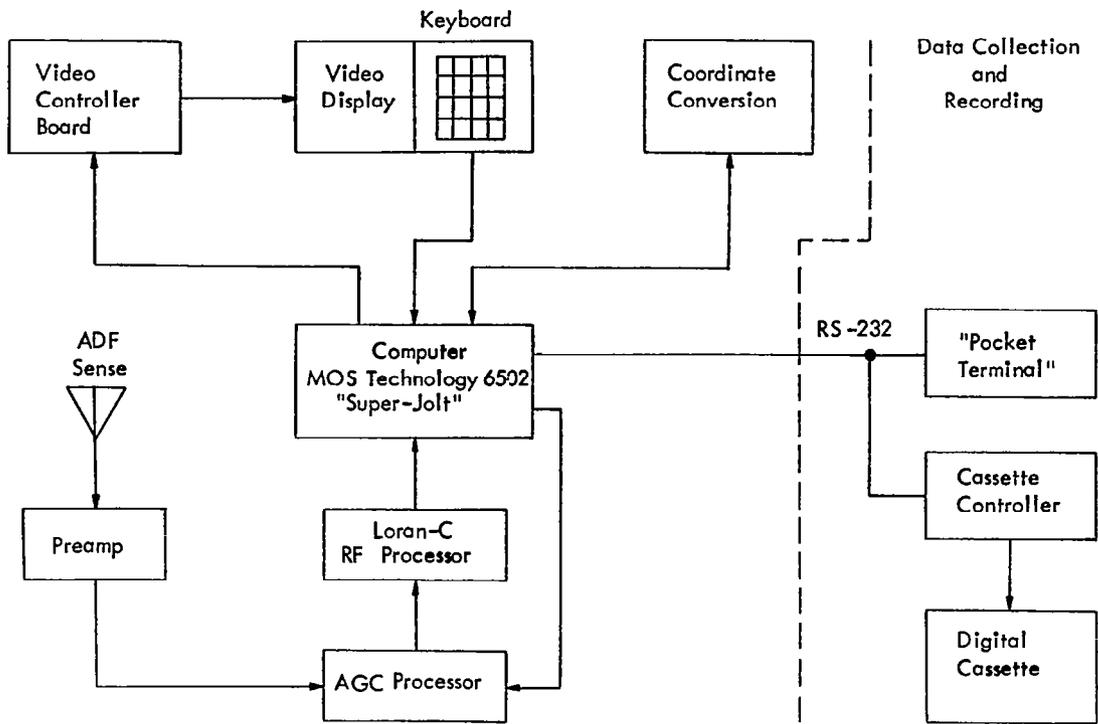


Figure 1. Prototype Loran-C receiver - block diagram.

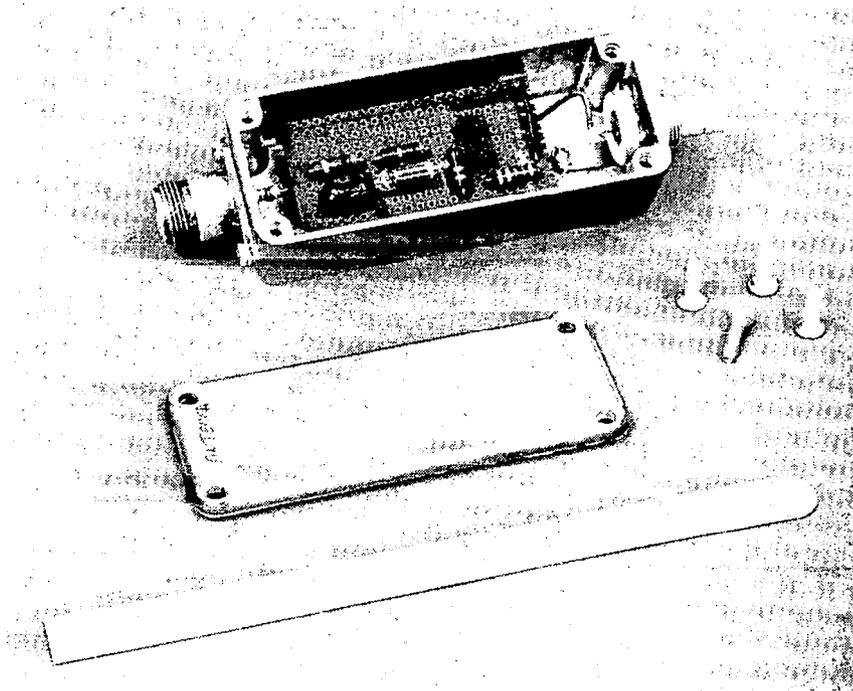


Figure 2. Wideband antenna preamplifier/coupler.

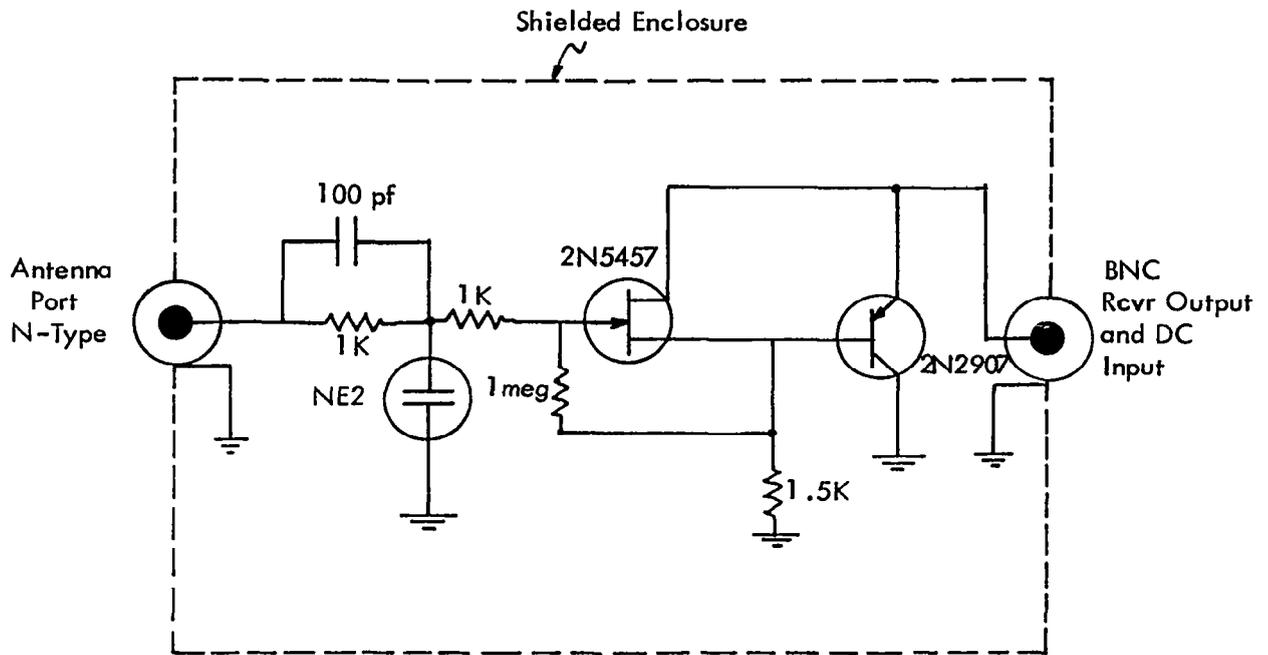


Figure 3. Preamplifier schematic.

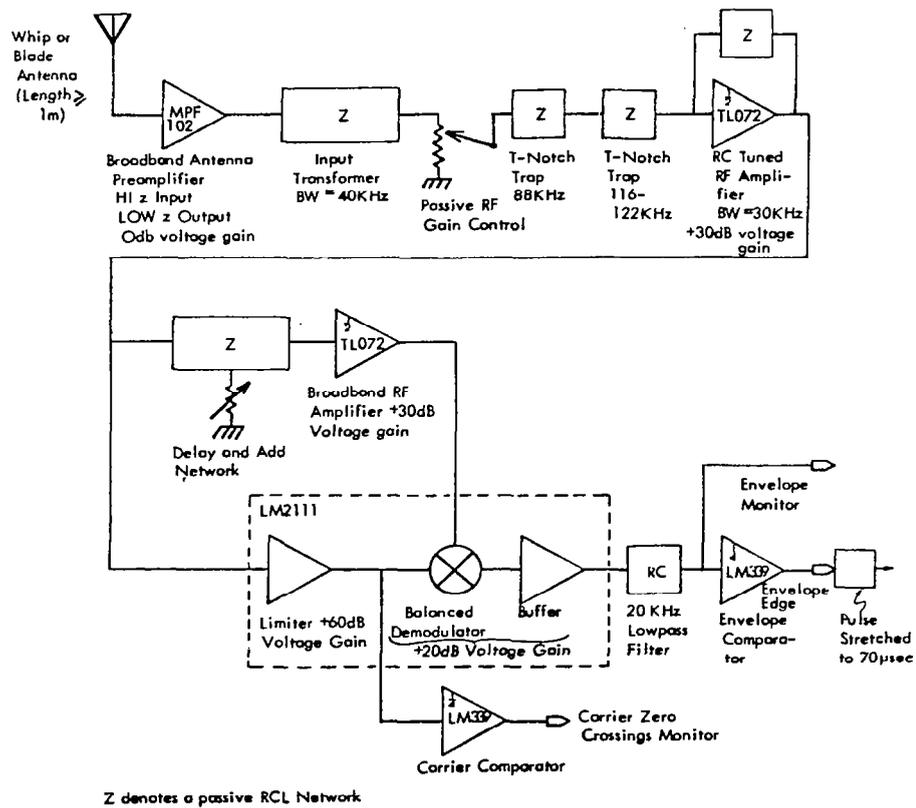


Figure 4. Loran-C autocorrelation envelope detector.

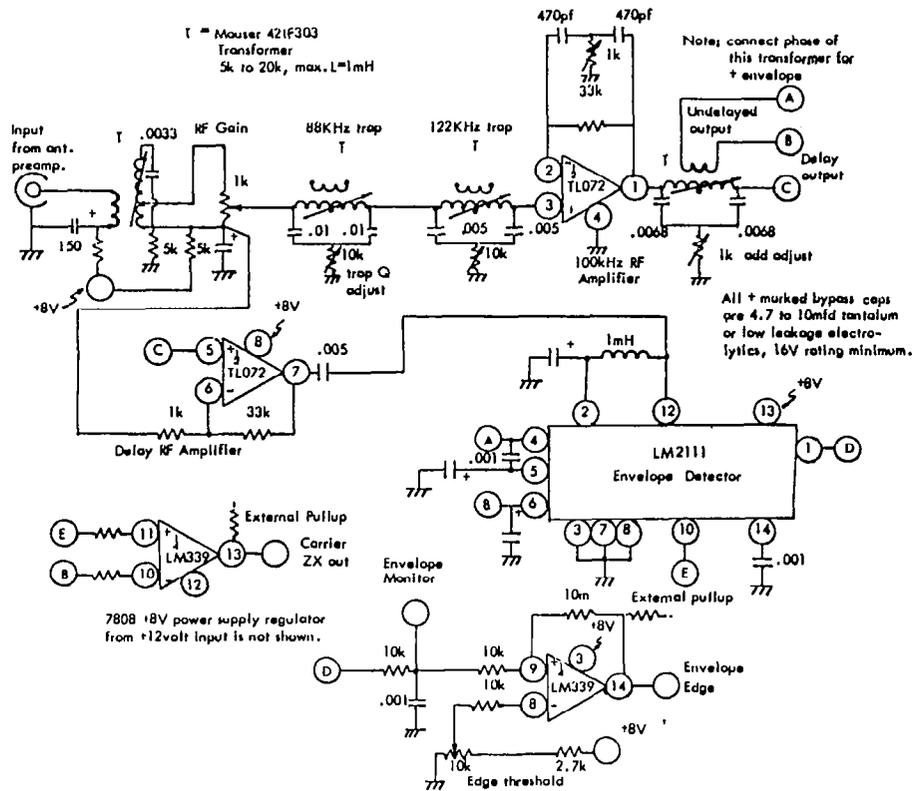


Figure 5. Mini-L80 Loran-C detector circuit.

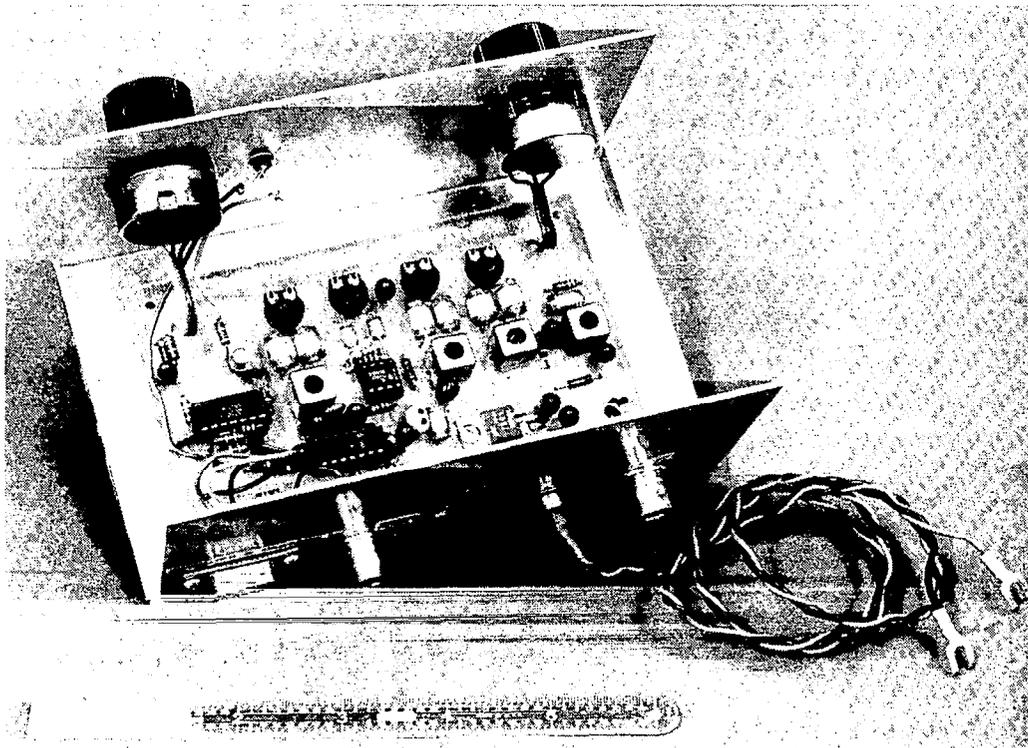


Figure 6. Prototype Loran-C RF processor.

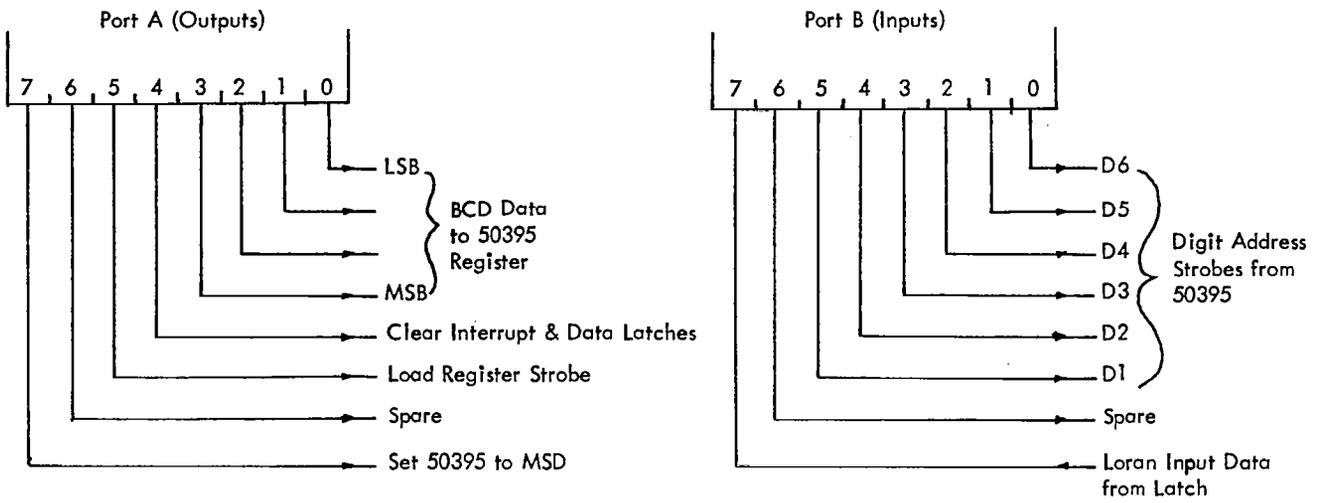


Figure 9. Tracking loop PIA assignment.

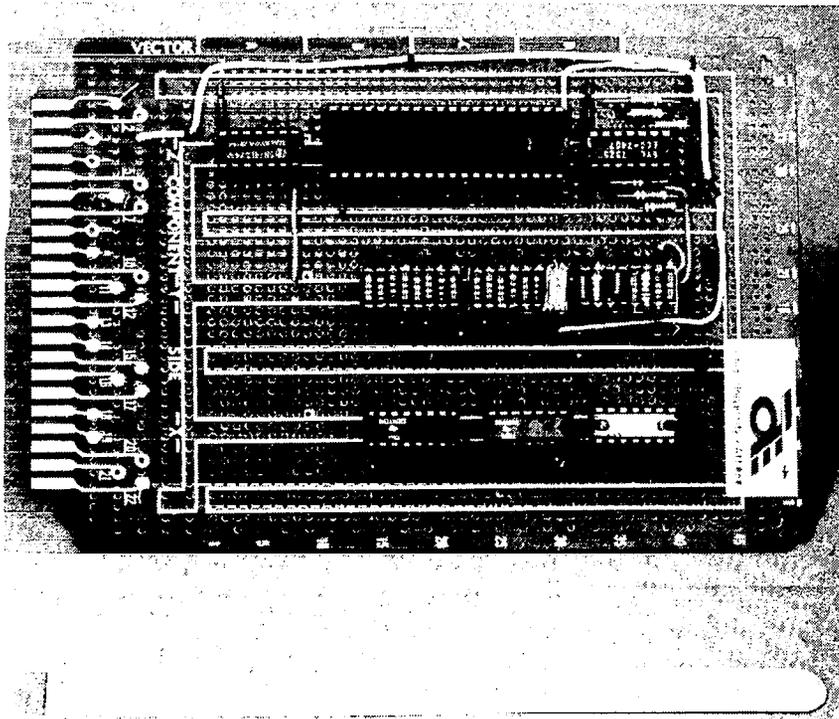


Figure 10. Tracking loop implementation.

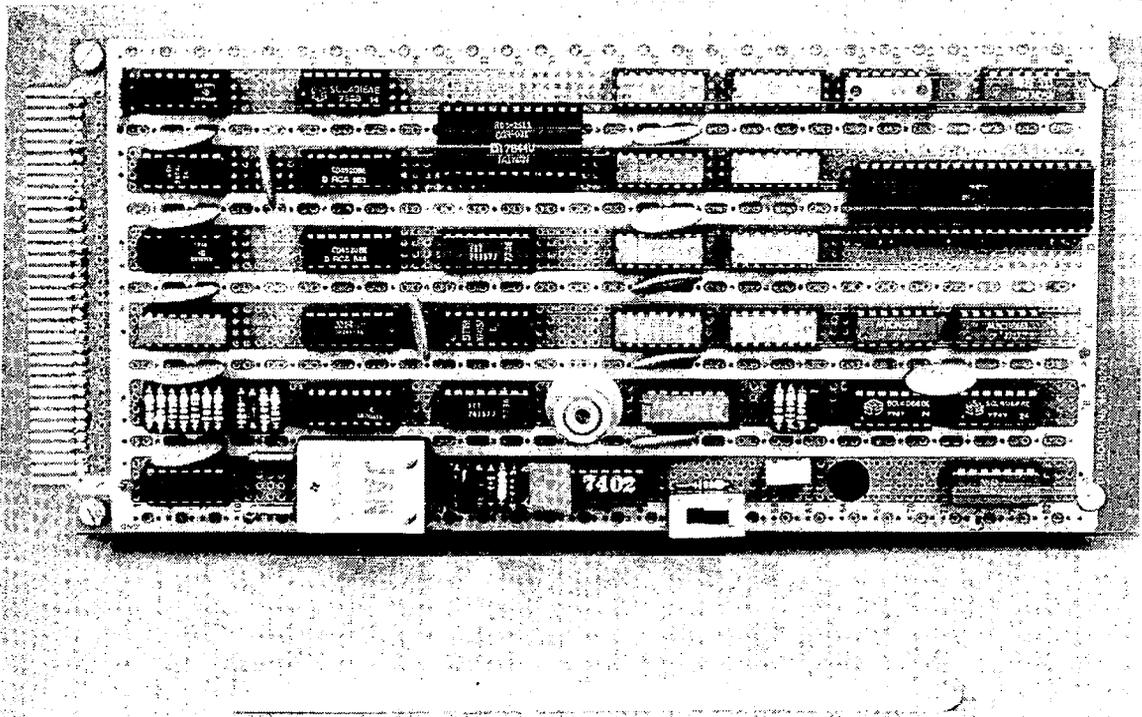


Figure 11. Video interface circuit board.

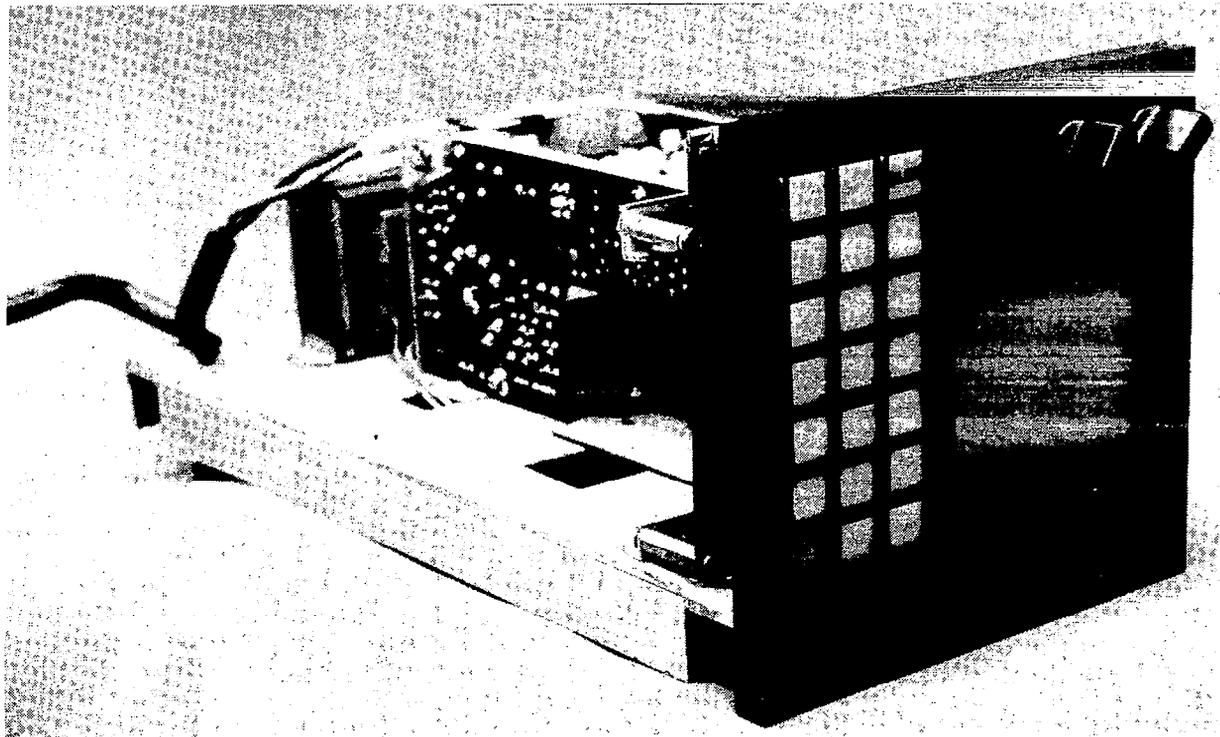


Figure 12. Receiver enclosure.

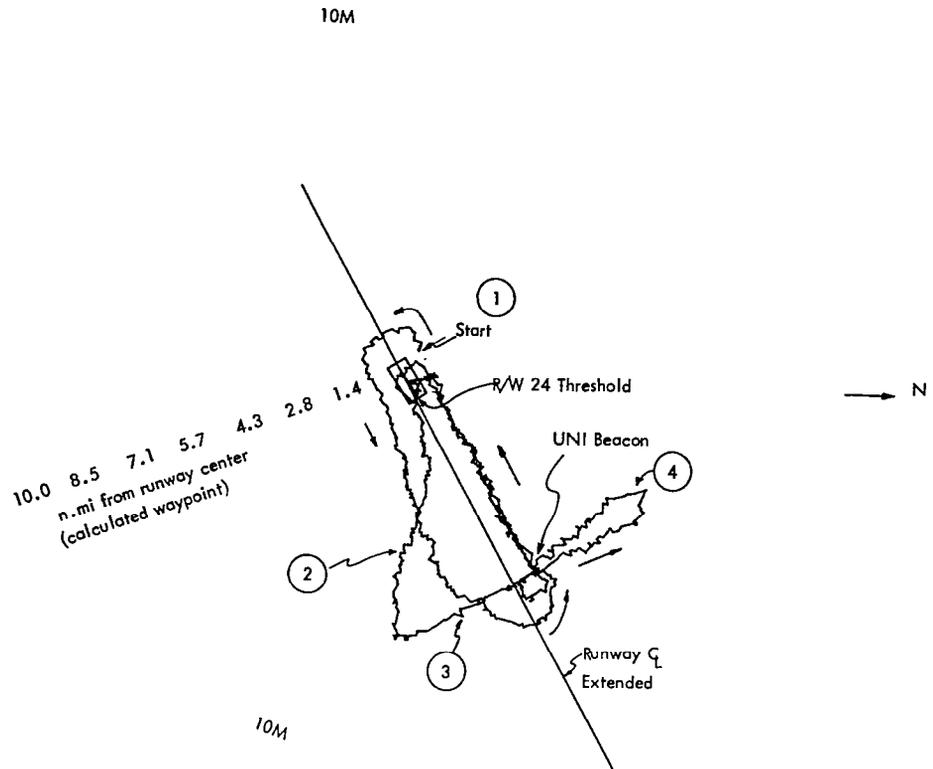


Figure 13. Flight test, Loran-C receiver prototype, March 9, 1981.

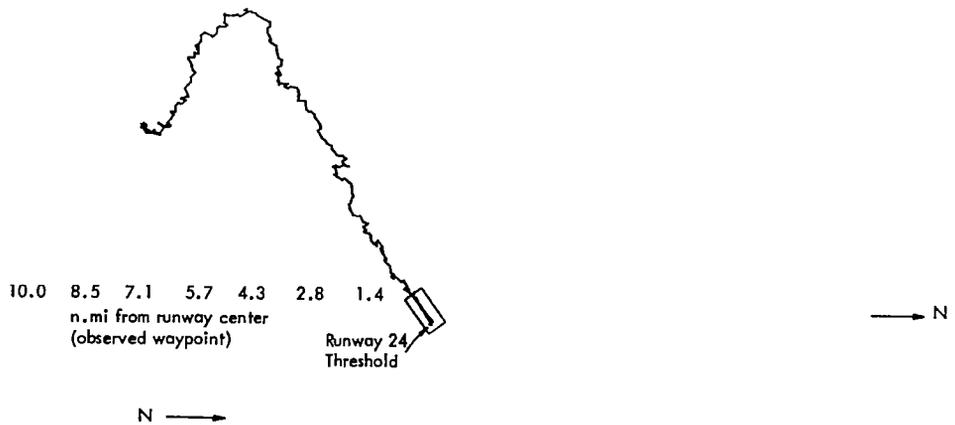


Figure 14. Flight test, Loran-C receiver prototype, March 9, 1981.
Ohio University Airport, PA-28-180, N56241, 99600 GRI.

TECHNICAL MEMORANDUM OU NASA' 81

COMMUTATED AUTOMATIC GAIN CONTROL SYSTEM

A commutated AGC system for the Ohio University prototype Loran-C receiver is described. The circuit design, fabrication, and test results are presented in this paper.

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I. INTRODUCTION

This technical memorandum deals with the commutated automatic gain control (AGC) system that has been designed and built for the Ohio University prototype Loran-C receiver (refer to Figure 1). The current version of the prototype receiver, the Mini L-80, was tested initially in the summer of 1980. The receiver uses a Microcomputer Associates™ Super Jolt microcomputer to control a memory-aided phase-locked loop (MAPLL). The microcomputer also controls the input/output, latitude/longitude conversion, and the recently added AGC system. (For a more detailed description of the receiver operation see ref. 1.)

The Ohio University receiver uses an envelope generator and zero crossing detector to produce a "Loran pulse" which is used by the MAPLL to track the Loran station. It was observed that significant errors in the time differences occurred when very strong or weak stations were included in the Loran chain being tracked (ref. 2). Experiments with a Loran simulator revealed that this error was caused by a phase shift and that this phase shift was due solely to the signal-to-signal ratio of the stations being tracked. For example, a 10 dB signal-to-signal difference produced approximately a 10 microsecond error while a 20 dB difference produced approximately a 25 microsecond error. (These results were obtained with an Epsco Loran simulator.)

To reduce or eliminate this error, a commutated AGC was proposed at the December 1980 NASA Joint University Program meeting (ref. 3). (See Figure 2.) The AGC samples the peak of the envelope for each station and stores the resulting voltage on a capacitor. This stored voltage is then used to control the gain of the input RF signal. The microcomputer switches the AGC sample from station to station. This paper describes the circuit designed for the AGC and will also present bench and flight test results. The AGC circuit described actually samples starting at a point 40 microseconds after a zero crossing determined by the software lock pulse ultimately generated by a 30 microsecond delay and add network in the receiver front-end envelope detector. Thus this sample point will be at about the peak of the ground wave signal and not necessarily at the peak of the envelope delayed by strong skywave contamination. Throughout this report the reference to "peak of the envelope" has this restricted meaning. The whole idea of AGC control is to adjust the level of each station signal such that the early portion of each envelope rise is about at the same amplitude in the receiver envelope detector.

The final design is an expansion of the original proposed design. (refer to block diagram Figure 3, as well as Figures 4, 5, and 6.) It consists of three major parts: A) The sample circuit, B) the DC gain circuit and, C) the AGC amplifier circuit.

II. SAMPLE CIRCUIT

The sample circuit is a two-stage sample-and-hold system with three separate channels; the switching of these channels is controlled by the

microcomputer. All integrated circuits are CMOS, and the supply voltage is +12 volts. This supply voltage is necessary because the sample voltage levels are in the range of 5 to 7 volts. It is important to note that this design has not yet been optimized for minimum chip count.

The amplitude of a station's envelope varies with that station's signal strength (refer to Figures 7 and 8). The two cascaded 4047 monostables create a delayed pulse to sample the peak of the envelope. The first 4047 triggers on the equals pulse (zero crossing; refer to Figure 9), and delays 40 microseconds. The second 4047 triggers on the negative edge of the 40 microsecond delay output and produces a 20 microsecond sample pulse (refer to Figure 10). The delay and duration of the sample pulse is optimized to sample the peak of the envelope for the weak as well as the strong station.

The envelope from the RF front-end is passed through a voltage follower, $1/2$ LM353, and into the 4051 analog demultiplexer. The 4051 has on-chip address decoding; therefore, the two control lines are decoded to:

0	0	search mode
0	1	channel one on
1	0	channel two on
1	1	channel three on

Note that the control lines are ANDed with the sample pulse so that each channel samples the peak of only one station's envelope. Each Loran station consists of eight pulses, and, therefore, the station is actually sampled eight times (refer to Figure 11). These eight 20 microsecond sample pulses are of sufficient duration to charge the 25 microfarad capacitor to the desired final value (the voltage of the peak of the envelope). Each station is sampled on a separate AGC channel every group repetition interval (GRI). The 4016 analog switch is configured for the negative of the logic of the 4051; therefore, the two- to three-line decoder is needed. The 4016 controls the "hold" for each channel. When a receiver channel is on, the corresponding switch for that channel in the 4016 is off. This allows the first stage capacitor to be charged while a constant voltage from the previous GRI charge is outputted from the second stage capacitor to the AGC amplifier. The .68 microfarad capacitor in the second stage of the sample-and-hold is large enough to hold a constant voltage for .1 second, the maximum GRI value. The second 4051 is enabled in the same manner as the first 4051 except that it is not pulsed. In addition, a +5 volt signal is applied to the 00 channel on the second 4051 to serve as a receiver gain setting used during Loran-C station search. The multiplexed output of the AGC sample voltage is represented in Figure 12.

The software changes to implement the procedure outlined above are minimal since the receiver operating software tracks each station individually. When the microcomputer starts its search routine, the 00 channel is activated to output the constant +5 volt search voltage to the AGC amplifier. When all three stations are being tracked, the commutated AGC

is activated and the envelopes for each station are sampled separately. It is not important to identify which Loran-C station is on a certain AGC channel since the microcomputer provides the necessary synchronization as a function of basic receiver operation.

III. DC GAIN CIRCUIT

The three AGC sample voltages are equal to the peak voltages of the envelopes of their respective stations. Therefore, a strong station stores a higher sample voltage than a weak station. The voltage-controlled amplifier designed for this AGC system requires a higher control voltage to amplify the weak stations; therefore, an inverter circuit was designed for this purpose. The circuit actually has a two-fold purpose, inverting and increasing the gain of the sample voltages. An LM 353 dual op-amp was chosen for this circuit. Referring to Figure 5, one can see that one-half of the chip is used for a voltage follower while the other half serves as the gain/inverter. The trimpot on the input to the second op-amp controls the gain of the AGC output voltage while the other trimpot controls the DC level of the output. The adjustment of these trimpots for proper AGC operation will be explained in Section V of this report.

IV. AGC AMPLIFIER

The AGC amplifier utilizes a CA3028A differential cascade amplifier (refer to Figure 6). The accompanying circuit has been optimized for this particular AGC application. (Refer to ref. 4 for a complete circuit description as well as test results.)

V. OPERATION

As stated previously, the gain and DC level trimpots of the DC gain circuit must be adjusted properly for optimum AGC performance (refer to Figure 13). As this graph indicates, the best AGC amplifier performance lies in approximately the three to eight volt range. The adjustment procedure is as follows:

1. Set the gain to unity (adjust the 10K ohm trimpot to its full value),
2. Set the DC level to +8 volts and allow the receiver to track all three stations and,
3. Increase the gain from unity until the lowest AGC voltage is equal to approximately 4 volts.

The properly functioning AGC will be similar to Figure 14. This adjustment procedure outlined above allows for the use of different antenna-preamp combinations which may possess different DC components in the input RF. It is important to note that once the DC gain circuit is properly adjusted to match a certain antenna-preamp combination, it need not be adjusted further.

VI TEST RESULTS

The first test of the AGC system performance was the use of the Epsco Loran simulator to provide different signal-to-signal ratios and record the results. An example of such an experiment appears in Figures 15, 16, and 17. A 10-millivolt input signal was used, which is characteristic of the signal strengths encountered with "live" Loran signals. The GRI was set at 99,600 microseconds and the time differences (TD's) were set to resemble those received off the air at Clippinger Labs, Athens, Ohio (TDY=42,594.3 microseconds, TDZ=56,775.9 microseconds). These results are approximated, observed time differences:

<u>Figure #</u>	<u>Attenuation</u>	<u>AGC</u>	<u>TDY</u>	<u>TDZ</u>
15	none	on	42,594.5	56,776.0
17	20dB station Y	on	42,605	56,776
16	20dB station Y	off	42,622	56,776

CONCLUSION: The AGC has little or no effect on "perfect" Loran signals, meaning that there is no degradation of performance with the AGC in operation. Also, twenty dB of signal-to-signal difference is an extreme case which might be encountered only at the limit of a Loran coverage area.

Following a number of simulator tests, the receiver was tested with a live signal. The first step was to obtain an accurate value for the correct time differences as recorded at Clippinger Labs. The Loran chain used was the U.S. Northeast, GRI=99,600 microseconds. Four receivers were tested and the results are as follows:

<u>Receiver</u>	<u>TDY</u>	<u>TDZ</u>
Texas Instruments 9900	42,594.4	56,776.0
Trimble 10A	42,594.3	56,775.9
TDL 302	42,595	56,776
OU Mini L-80 (no AGC)	42,600	56,775

To obtain enough data points for a good statistical sample, sixty minutes of data was collected with the Ohio U. Loran receiver on October 20, 1981 from 4:00 to 5:00 p.m., thirty minutes without AGC, and thirty minutes with AGC. Each of these thirty-minute segments was broken into ten-minute blocks for a total of six blocks, 550 to 600 data points each. The atmospheric conditions were: light cloud cover with moderate spherics activity observed on an oscilloscope. A statistical analysis package available on Ohio University's IBM 370/158 was used to obtain the results shown in Figures 18 and 19. Most of the accuracy displayed is not significant but the trends are evident.

CONCLUSION: The addition of the AGC improved the value of TDY by approximately four microseconds. The overall accuracy of the receiver is approaching ± 1 microsecond. One point of special interest is the greater variance of TDY with the AGC on. This is due to the occasional sampling of cross-rate interference.

The most important test of a prototype navigation receiver is a flight test. Ohio University's DC-3 flying laboratory made two Loran data collection flights on August 29th and 31st, 1981. The flights were centered around south-central Ohio and in areas of light thunderstorm activity. The operational Loran receivers were: TI 9900, Trimble 10A, and O. U. Mini L-80. The results of the August 29th Columbus to Albany via Zanesville leg are presented graphically in Figure 20. (August 31st data is omitted from this report because the results are essentially the same.) The O. U. receiver data was hand-collected and it appears with the flight path plotted by the TI 9900.

CONCLUSION: The plot shows a very close alignment of the two paths. Note the slight (less than .5 nautical miles) north bias of the O. U. receiver path. These plots were obtained with latitude/longitude data and not time difference data. The latitude/longitude conversion employed in the O. U. receiver does not use any overland propagation delay corrections in the calculations. This bias is due mainly to lack of propagation delay correction rather than large time difference errors.

VII. CONCLUSIONS

The addition of AGC to the O. U. Loran-C receiver has improved the accuracy of the time difference calculations to within approximately \pm 1.5 microseconds of the observed time differences for a given position. This translates to an improvement of absolute accuracy of approximately 0.5 nautical mile. Tests of Ohio University's receiver with and without the AGC have indicated these results. The majority of error now present in the positional data supplied by the Ohio University receiver is due to the lack of propagation delay corrections.

Two additional refinements could improve the performance of the AGC system further: 1) a filter to reduce the effect of cross-rate interference on the sampling of the envelopes, and 2) an AGC amplifier with more dynamic range for an even greater signal-to-signal gain. Complete software control would eliminate the adjustments outlined in Section V, thus the receiver would require no manual gain adjustments. Other software development could allow for the tracking of all the Loran stations in a particular chain. The three most suitable signals would then be used to obtain positional data.

VIII. SUMMARY

A commutated automatic gain control system has been designed and constructed specifically for the Ohio University prototype Loran-C receiver. The AGC is designed to improve the signal-to-signal ratio of the received Loran signals. The AGC design does not require any analog to digital conversion and it utilizes commonly available components. The AGC system consists of three major parts: 1) the sample circuit, which samples the peak of the envelope of the Loran signal to obtain an AGC voltage for each of three Loran stations, 2) a DC gain circuit to control the overall gain of the AGC system, and 3) an AGC amplifier to amplify

the input RF signal. The performance of the AGC system has been observed in bench and flight tests and it has improved the overall accuracy of the Ohio University receiver considerably.

IX. ACKNOWLEDGEMENTS

The design, construction and testing of the commutated AGC system has been funded by the NASA Joint University Program for Air Transportation Research as a part of the continuing development of Ohio University's prototype Loran-C receiver. The author would like to thank Dr. Robert Lilley and Mr. Ralph Burhans, both project engineers, for their help in the design of the AGC. James Nickum, Avionics Engineering Center engineer, helped with the data collection, especially the flight testing. He also took all of the photographs that appear in this paper. Research interns Stan Novacki, James Roman and David Bernard were also of assistance in various phases of this project.

X. REFERENCES

1. Lilley, Dr. R.W. and Daryl McCall, "A Loran-C Prototype Navigation Receiver for General Aviation", OU NASA TM-80, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio 45701, August 1981. (Pages 121-137 of this compilation.)
2. Fischer, Joseph P., "Results of a Loran-C Flight Test Using an Absolute Data Reference", OU NASA TM-74, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio 45701, January 1980.
3. "Joint University Program for Air Transportation Research - 1980", NASA CP-2176, Langley Research Center, December 1980.
4. Roman, James P., "Automatic Gain Control", OU NASA TM-79, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio 45701, March 1981. (Pages 115-119 of this compilation.)

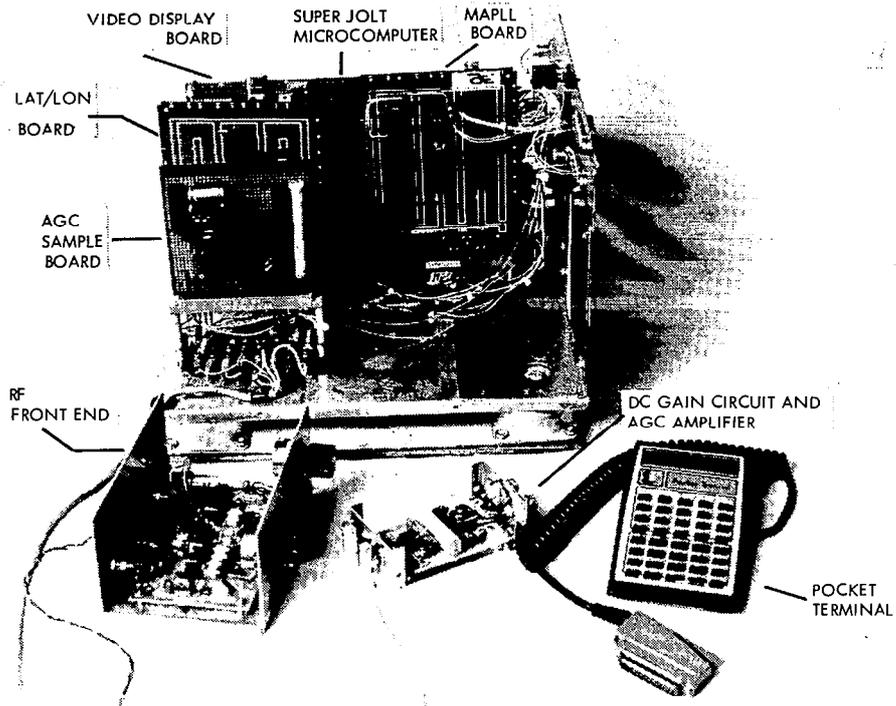
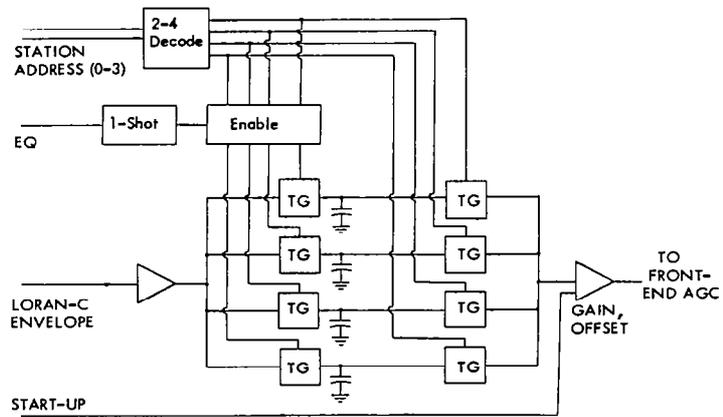


Figure 1. Ohio University Loran-C receiver.



LORAN-C RECEIVER COMMUTATED AGC

- To be Added to Loran-C Low-Cost Prototype
- Commutated, Sampled AGC
- Avoids Front-End Phase Shift Problem
- Five Chips Required for Breadboard
- Permits Present AGC for Search Mode
- Minimum Load on Computer

Figure 2. Proposed commutated AGC.

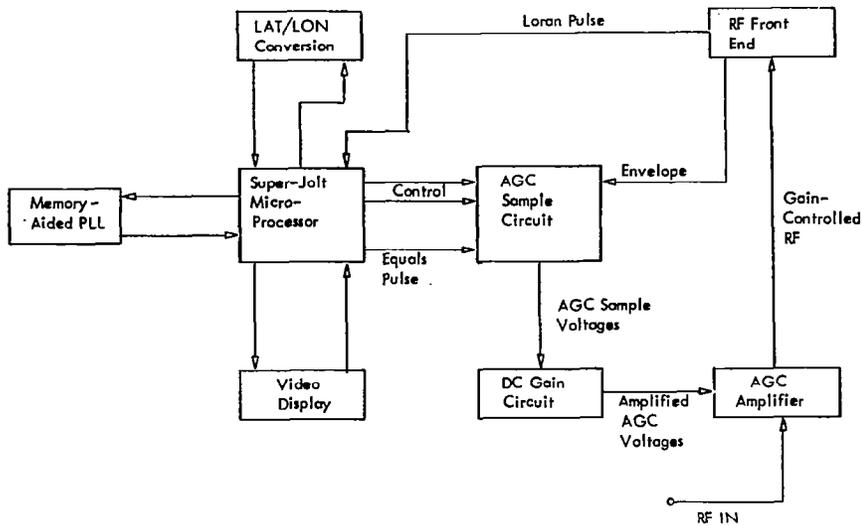


Figure 3. Ohio University Loran-C receiver block diagram with AGC.

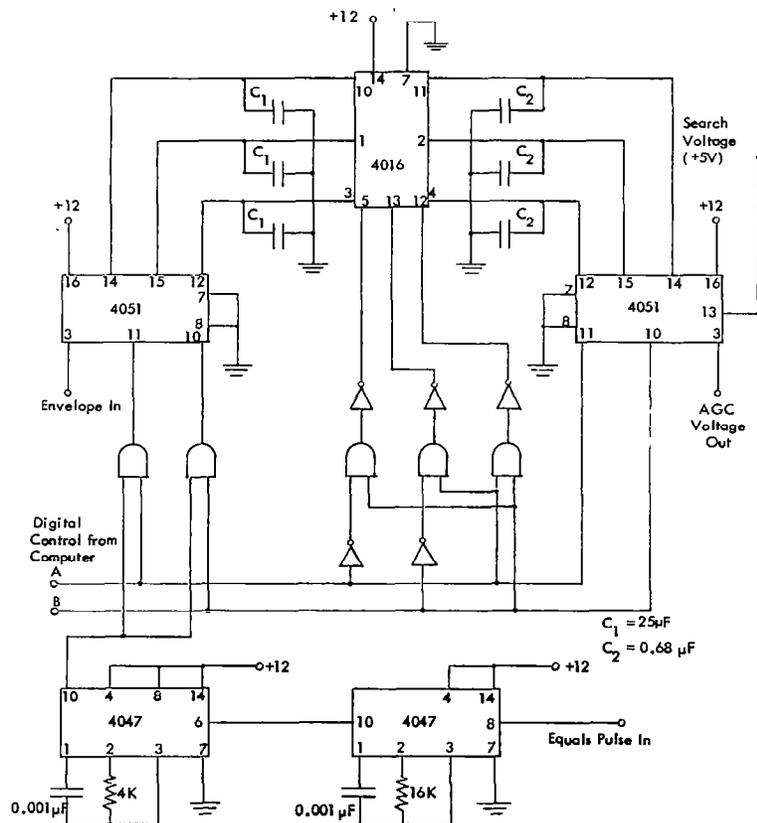


Figure 4. Schematic of the commutated AGC circuit designed for the Ohio University Loran-C receiver. All of the IC's are CMOS. This circuit is designed to sample the peak of the envelope of a Loran pulse to obtain an AGC voltage.

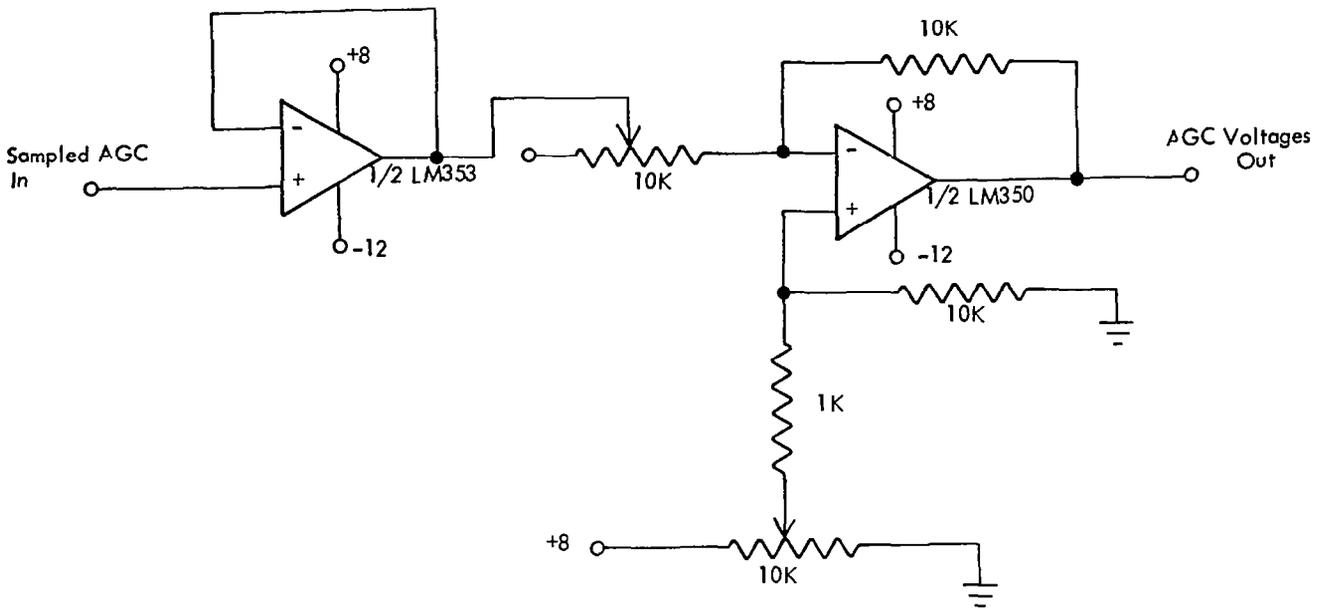


Figure 5. DC gain circuit.

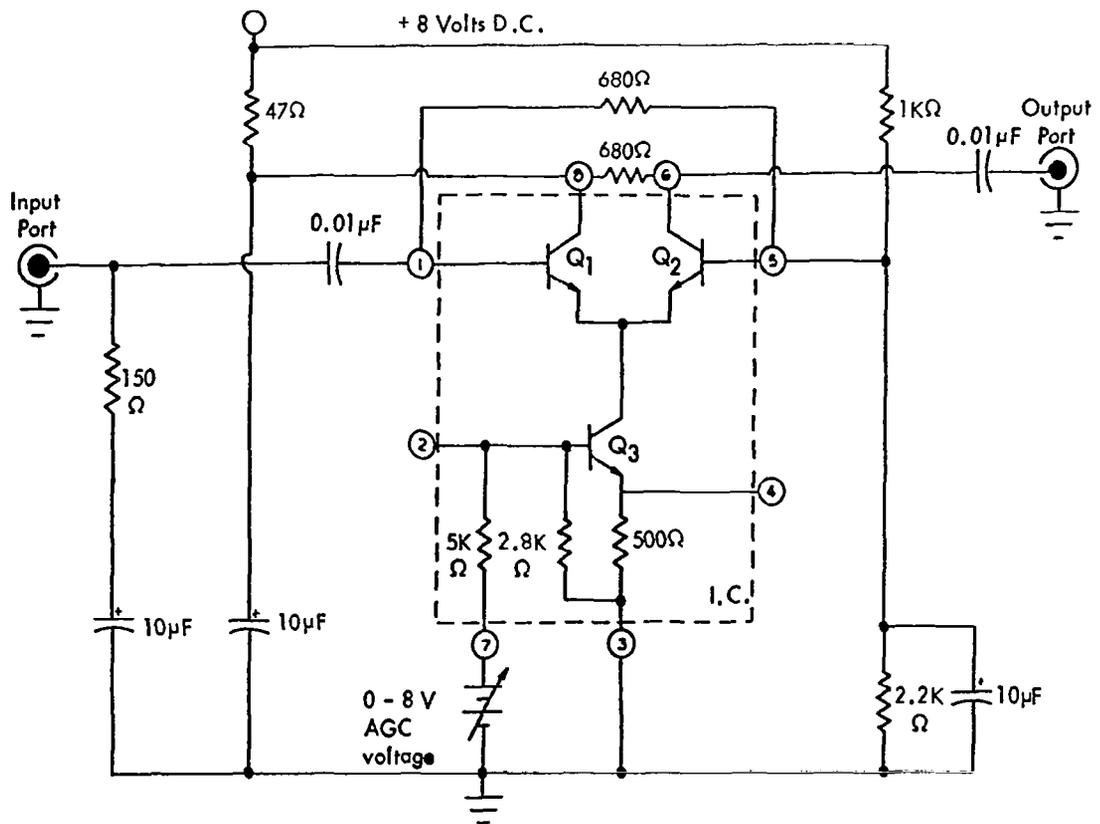


Figure 6. Automatic gain control circuit (amplifier only).

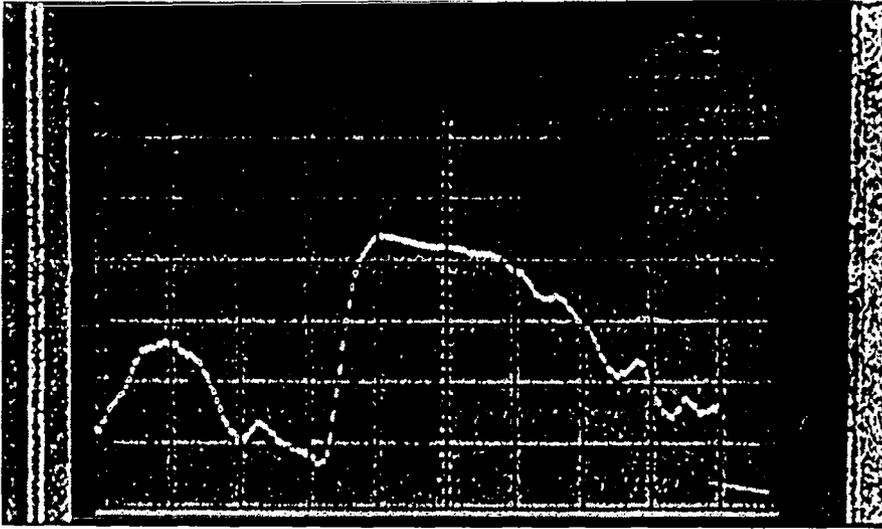


Figure 7. Strong station envelope. Live signal, M station (Seneca, NY).

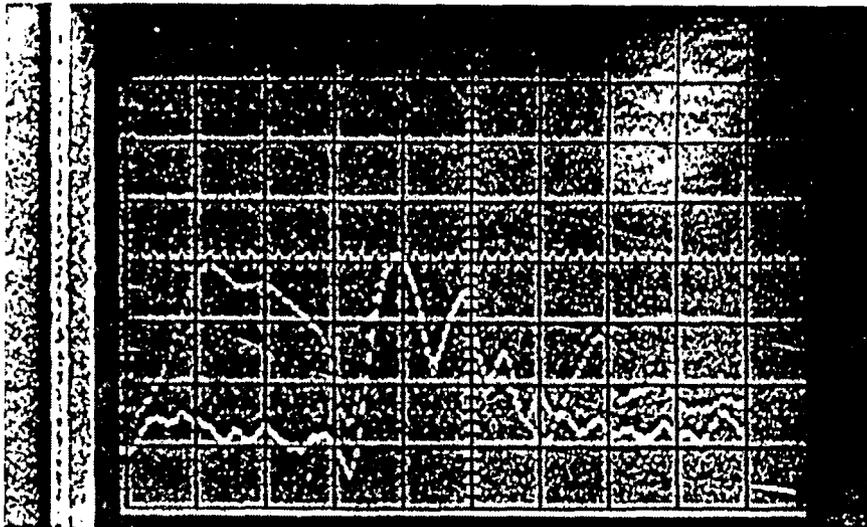


Figure 8. Weak station envelope. Live signal, Y station (Carolina Beach).

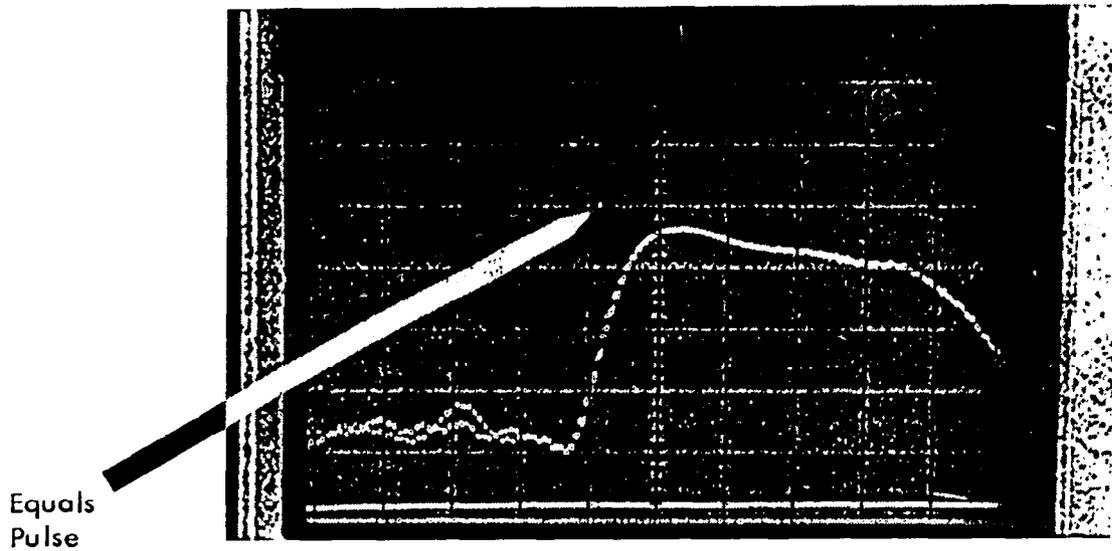


Figure 9. One μsec equals pulse at zero crossing.

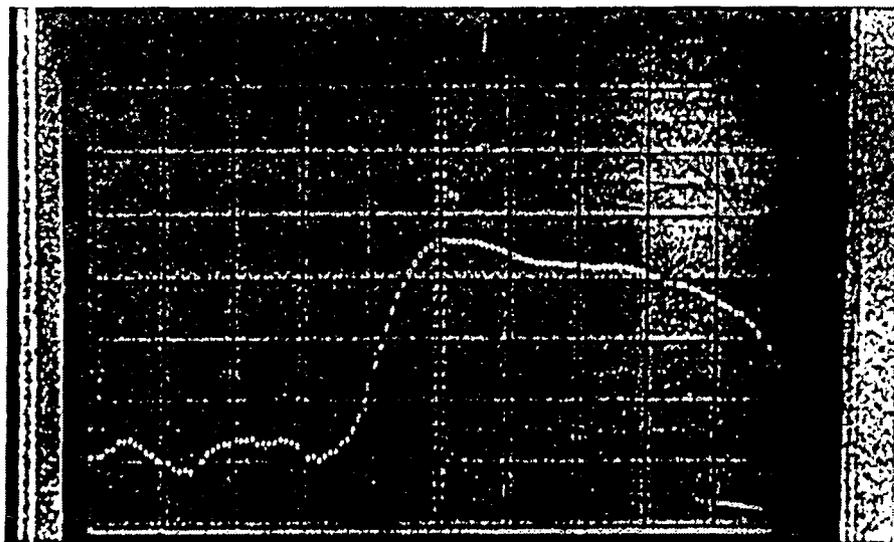


Figure 10. Twenty- μsec sample pulse at peak of envelope.

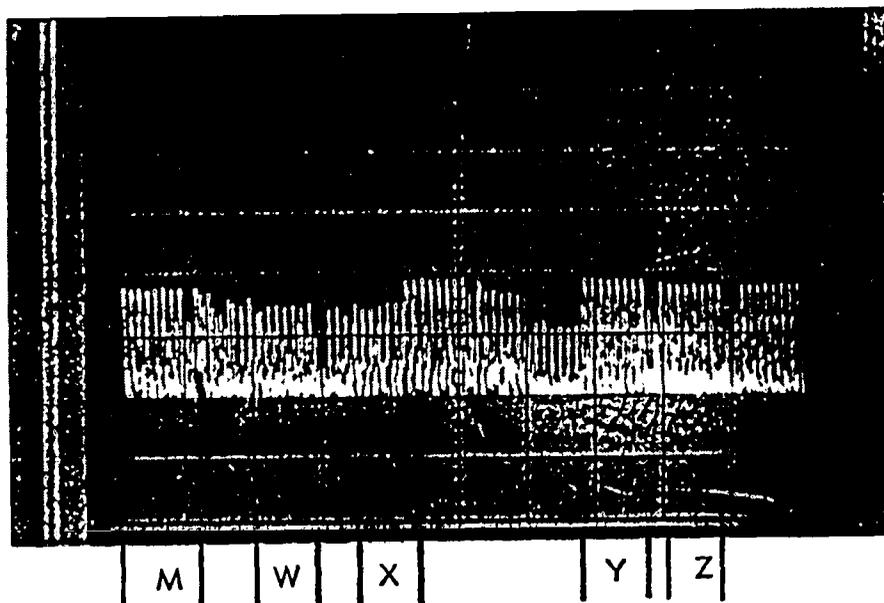


Figure 11. Loran chain as received at Clippinger Labs.
 GRI = 99600 μ sec. Note cross-rate interference.

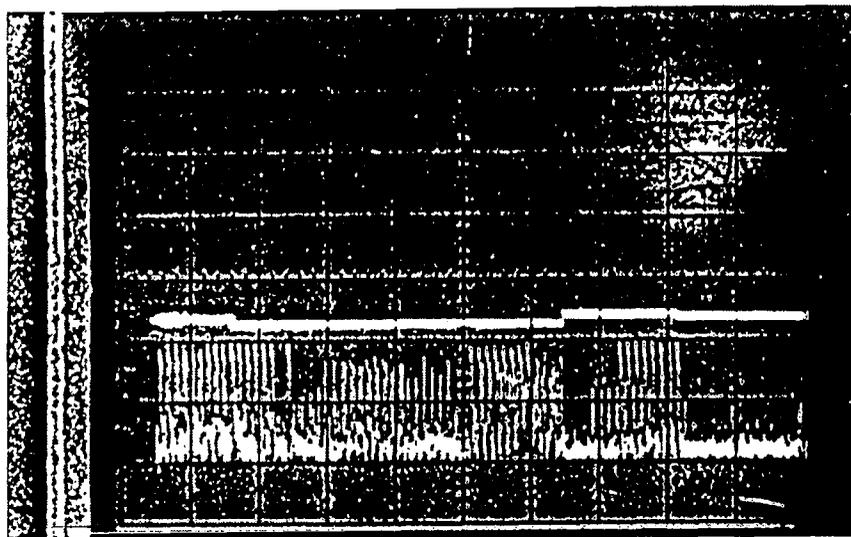


Figure 12. AGC sample voltages.

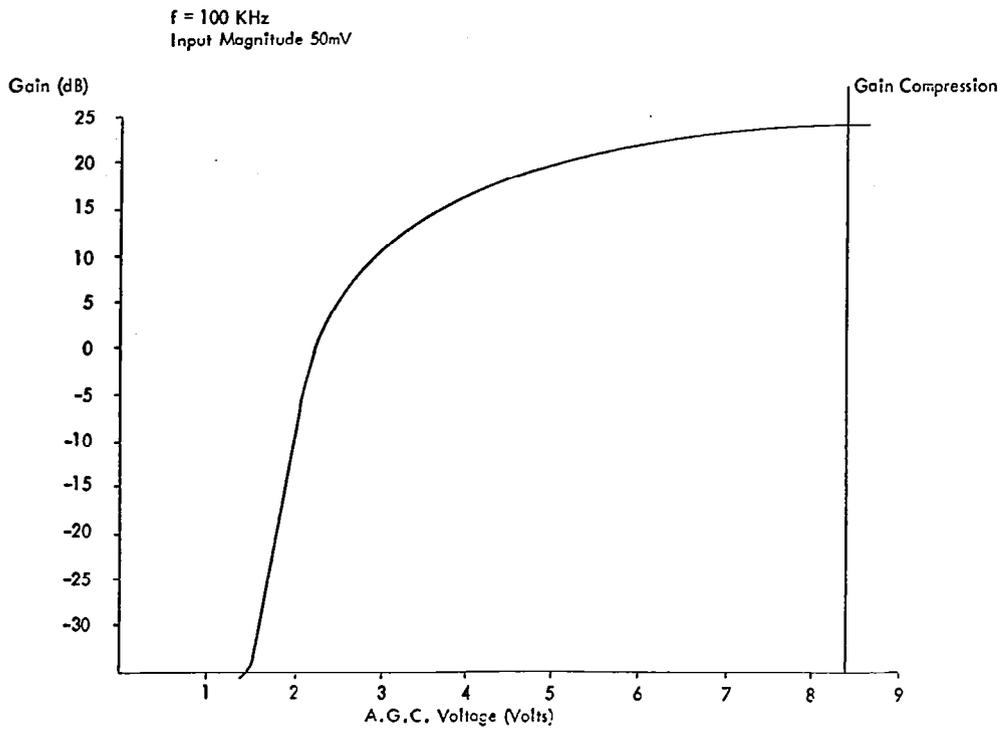


Figure 13. AGC amplifier performance curve.

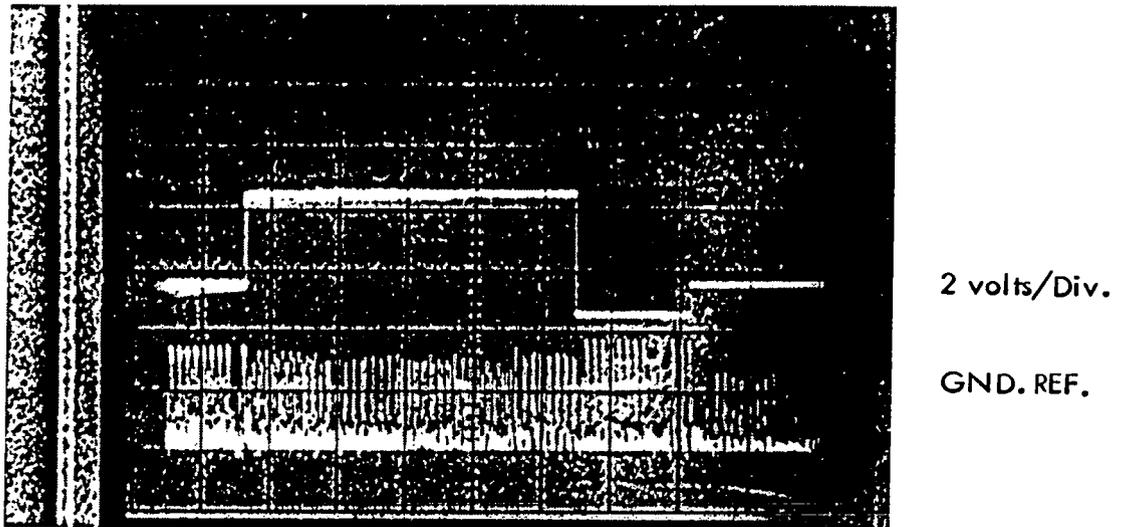
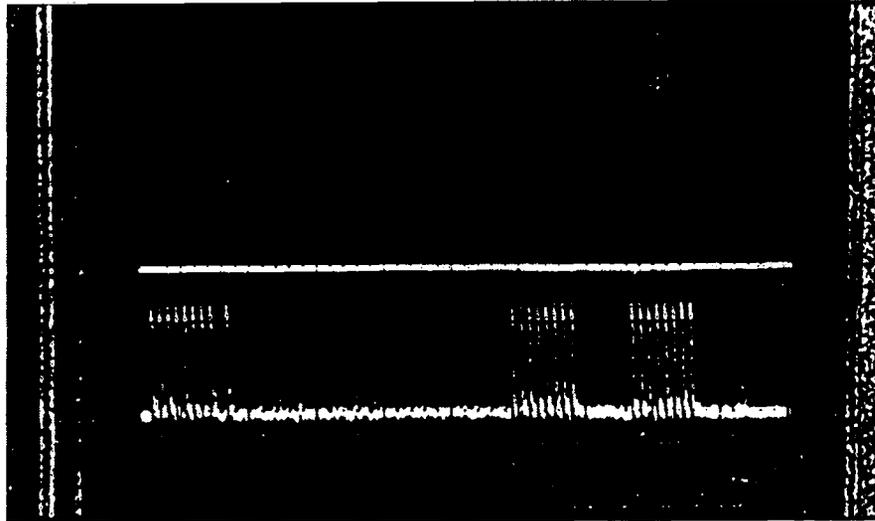


Figure 14. AGC voltages, live signal.



2 volts/Div.

GND REF.

Figure 15. Ten-mV signal on simulator, no station attenuation, AGC on.

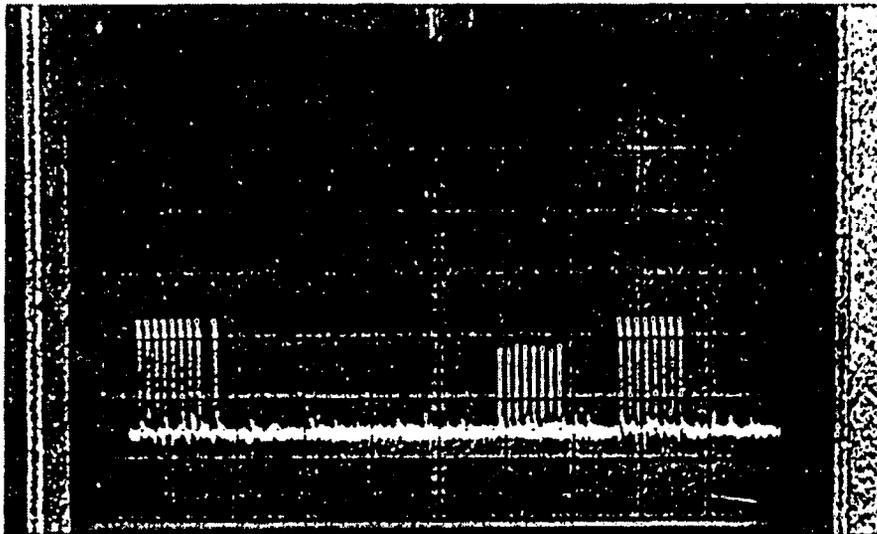
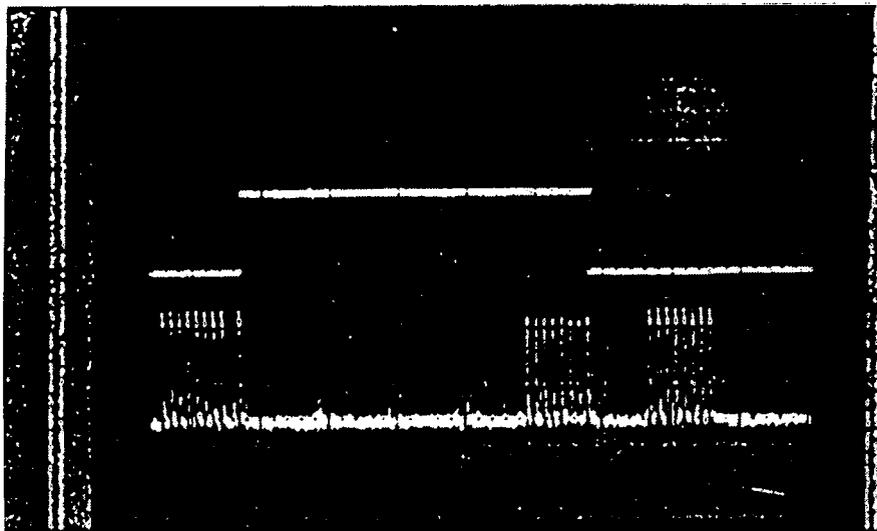


Figure 16. Ten-mV signal, 20 dB attenuation on station Y, AGC off.



2 volts/Div

GND. REF.

Figure 17. Ten-mV signal, 20 dB of attenuation on station Y, AGC on. Note improvement from Figure 16.

AGCTEST1					14:25 FRIDAY, NOVEMBER	
MEAN	STANDARD DEVIATION	MINIMUM VALUE	MAXIMUM VALUE	STD ERROR OF MEAN	SUM	VARIANCE
42599.4002347	0.51903853	42597.700000	42601.300000	0.02514750	18147344.500	0.26940039
56775.3119718	0.52392441	56773.600000	56776.700000	0.02538422	24166282.900	0.27449678

AGCTEST1					14:25 FRIDAY, NOVEMBER	
MEAN	STANDARD DEVIATION	MINIMUM VALUE	MAXIMUM VALUE	STD ERROR OF MEAN	SUM	VARIANCE
42599.4434109	0.49396906	42597.900000	42600.900000	0.02174578	21981312.800	0.24400543
56775.3350775	0.44001746	56774.100000	56776.600000	0.01937069	29296072.900	0.19361537

AGCTEST1					14:24 FRIDAY, NOVEMBER	
MEAN	STANDARD DEVIATION	MINIMUM VALUE	MAXIMUM VALUE	STD ERROR OF MEAN	SUM	VARIANCE
42599.7463659	0.42819454	42598.500000	42601.000000	0.02143654	16997298.800	0.19335057
56775.3644110	0.40127825	56774.200000	56776.500000	0.02008904	22653370.400	0.16102424

Figure 18. Bench test results without AGC.

AGCTEST1					14:15 FRIDAY, NOVEMBER	
MEAN	STANDARD DEVIATION	MINIMUM VALUE	MAXIMUM VALUE	STD ERROR OF MEAN	SUM	VARIANCE
42596.2689342	0.61590858	42594.600000	42597.800000	0.02932898	18784954.600	0.37934338
56776.9875283	0.44090975	56775.700000	56778.100000	0.02099570	25038651.500	0.19440141

AGCTEST1					14:14 FRIDAY, NOVEMBER	
MEAN	STANDARD DEVIATION	MINIMUM VALUE	MAXIMUM VALUE	STD ERROR OF MEAN	SUM	VARIANCE
42596.0725979	0.59603481	42594.600000	42597.400000	0.02514221	23938992.800	0.35525749
56776.9188612	0.43206040	56775.700000	56777.900000	0.01822537	31908628.400	0.18667619

AGCTEST1					14:13 FRIDAY, NOVEMBER	
MEAN	STANDARD DEVIATION	MINIMUM VALUE	MAXIMUM VALUE	STD ERROR OF MEAN	SUM	VARIANCE
42595.5914894	0.87943572	42592.300000	42597.700000	0.03867754	22021920.800	0.77340719
56776.7504836	0.42543371	56775.400000	56777.900000	0.01871055	23353530.000	0.18099384

Figure 19. Bench test results with AGC.

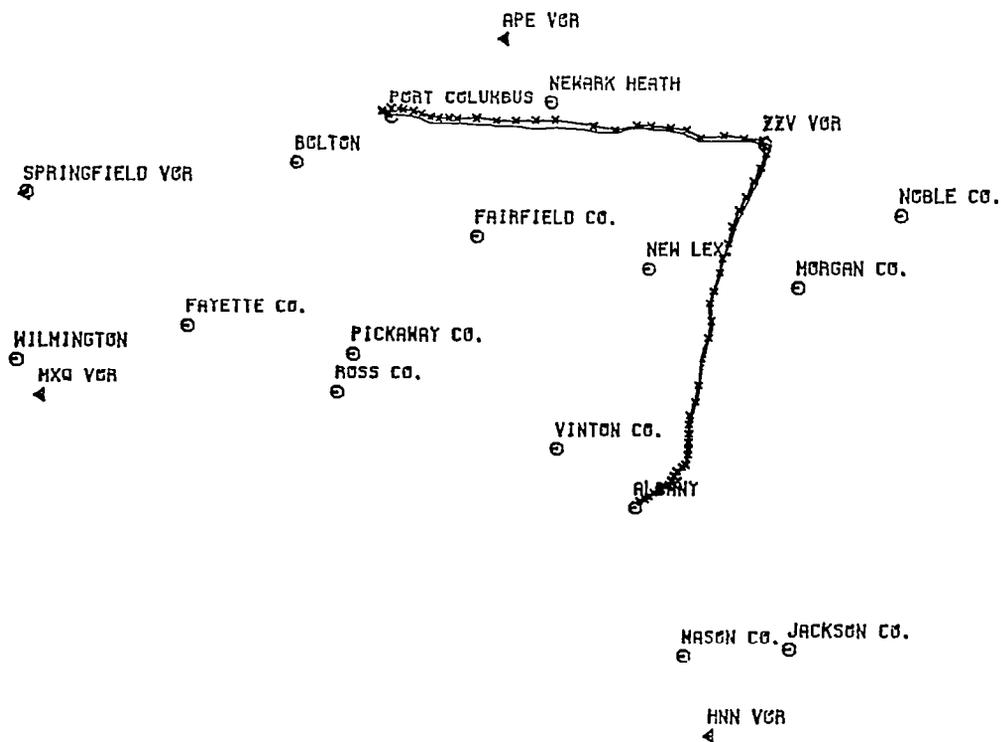


Figure 20. DC-3 flight test, 29 August 1981. TI-9900 flight path is the solid line. OU Loran-C is the line with X's. Note the slight north bias of the OU Loran-C data.



TECHNICAL MEMORANDUM OU NASA' 82

A PROTOTYPE INTERFACE UNIT FOR
MICROPROCESSOR-BASED LORAN-C RECEIVER

A command entry and display device designed to allow convenient operation of the Loran-C receiver-processor is described.

Stanley M. Novacki III

Avionics Engineering Center
Department of Electrical Engineering
Ohio University
Athens, Ohio 45701

I. INTRODUCTION

This paper documents an inexpensive data/command entry and display system being developed by the Ohio University Tri-University group. This system is designed to operate in place of a separate ASCII terminal. Also described is the software to interface this unit to the 6502-based navigation receiver currently under development at Ohio University.

II. HARDWARE IMPLEMENTATION

See Figure 1 for an overview of the command entry and display logic. In order to retain the use of some of the DEMON(TM) monitor facilities provided by the SuperJOLT(TM) microcomputer, an ASCII encoded keypad consisting of the decimal digits, decimal point, and nine letters has been designed as shown in Figure 2. A printed circuit board was prepared to produce the appropriate X-row Y-column code appropriate for each character (Figure 3). This X-Y code is input to a General Instruments AY-5-2376 keyboard encoder [1]. Figure 4 shows the encoder along with an NEC μ 8212 octal latch, which stores the value of the pressed key until the microprocessor can poll the keyboard and read the data.

The latch holding the 7 bits of character data and a key-pressed strobe is made available to a 6530 Versatile Interface Adapter (VIA) on the J2 connector of the SuperJOLT microcomputer. Port A of the 6530 is configured as an input: lines 0 through 6 carry the ASCII value of the key, line 7 the key-pressed strobe which acts as a flag during the polling process to indicate that new data is present. Line 2 of the "B" port is set as an output line; after data has been read from the "A" port, line B2 is toggled to clear the latch so that new data can be read.

A Sony AVF-3250A 4-inch black-and-white monitor designed for 13 VDC operation was chosen for the display due to the ease with which it could be integrated into a standard avionics-size enclosure as shown in Figure 5. The monitor accepts standard NTSC composite video signals, requires 14 watts at 13 VDC and weighs approximately 1.9kg.

The VDM-1 Video Display Module [2] allows for the use of alpha- numerics and graphic primitives in a 16x16 format along with a 256 x 256 coarse graphics mode and a 512 x 512 high resolution mode. This versatility allows for a variety of alphanumeric, graphic, or combined-mode displays. Such capabilities allow for receiver output to be displayed in CDI, HSI, or other analog data formats easily recognized and interpreted by the pilot.

III. SOFTWARE INTERFACE

A monitor routine is being written in 6502 assembly language to perform data input and output between the command/display unit and the

SuperJOLT microcomputer. The DEMON(TM) monitor routine can provide all services necessary for system initialization and data input; however, it also requires a full communications terminal and does not offer the range of display formats offered by the VDM graphics unit. The attendant reduction in size and weight coupled with the ease of operation made possible by tailoring the monitor to a specific application make the development of a custom software interface highly desirable.

There are four tasks currently envisioned for the interface monitor. They consist of:

1. Selecting the mode of operation; for example, direct-route or multi-waypoint navigation.
2. Provide user prompts for the data input needed for the specified mode of operation.
3. Provide data conversion from a user-oriented format to a microprocessor-oriented one.
4. Select the display mode of the processor output.

Tasks 1 and 2 are fairly obvious and no further elaboration will be given here. Data format conversion is required because the current versions of the time-difference to latitude-longitude and area navigation routines require information such as waypoint location to be given in a particular 32-bit floating-point format as used by the Advanced Micro Devices Am9511A arithmetic processor [3]. This format is illustrated in Figure 6. The format conversion typically consists of stripping the ASCII zone bits and performing a BCD-to-binary conversion and then "floating" the 8-bit integer number into the 32-bit format. This data format change is greatly simplified by the arithmetic facilities of the Am9511A: software multiply-and-add routines are replaced by presenting data to the math chip and giving it the appropriate operation codes. This decrease in the size of the interfacing software and attendant improvements in program legibility make software maintenance much easier, especially in terms of code optimization for faster execution as well as increased memory resources to allow for more sophisticated I/O routines.

Perhaps the most significant difference between the interface monitor and the terminal monitor is that the former cannot be interrupt driven. The processor's principal function is monitoring the LORAN-C pulse train and deriving time-differences from them to drive the navigation routines. An interrupt to service something as irrelevant to the pulse tracking and TD measurements as a change of display formats would force the receiver to retrack the pulse trains, reducing the total time the processor is devoting to actual navigation duties. As an extension of the data display currently used in the prototype receiver, the keyboard will be polled as part of the general housekeeping software. The information from the keypad is stored until the processor has the opportunity to implement the command.

IV. SUMMARY

An ASCII keypad with a CRT display capable of alphanumeric and graphics-mode operation is being developed to provide specialized data entry and display for the Ohio University LORAN-C receiver/processor. This unit is being developed to replace conventional communications terminals so as to simplify receiver operations to a level typical of current avionics systems.

V. REFERENCES

- [1] KBD-5 Keyboard and ASCII Encoder, Southwest Technical Products, San Antonio, Texas, 1978.
- [2] VDM-1 Video Display Module, Microcomputer Products Co., Columbus, Ohio, 1980.
- [3] Am9511A MOS/LSI Arithmetic Processor, Advanced Micro Devices, Sunnyvale, California, 1979.

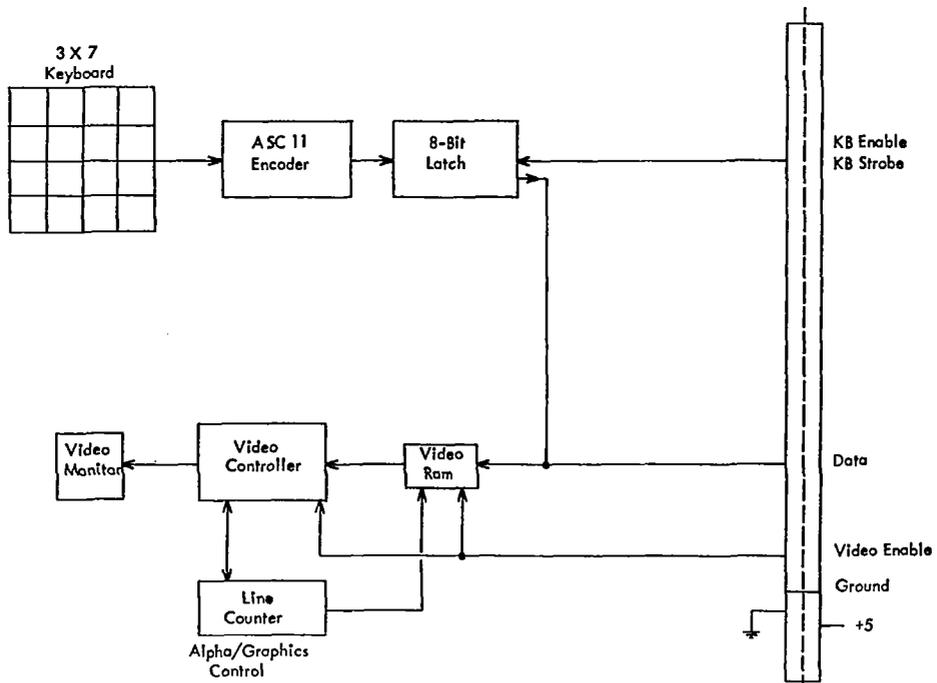


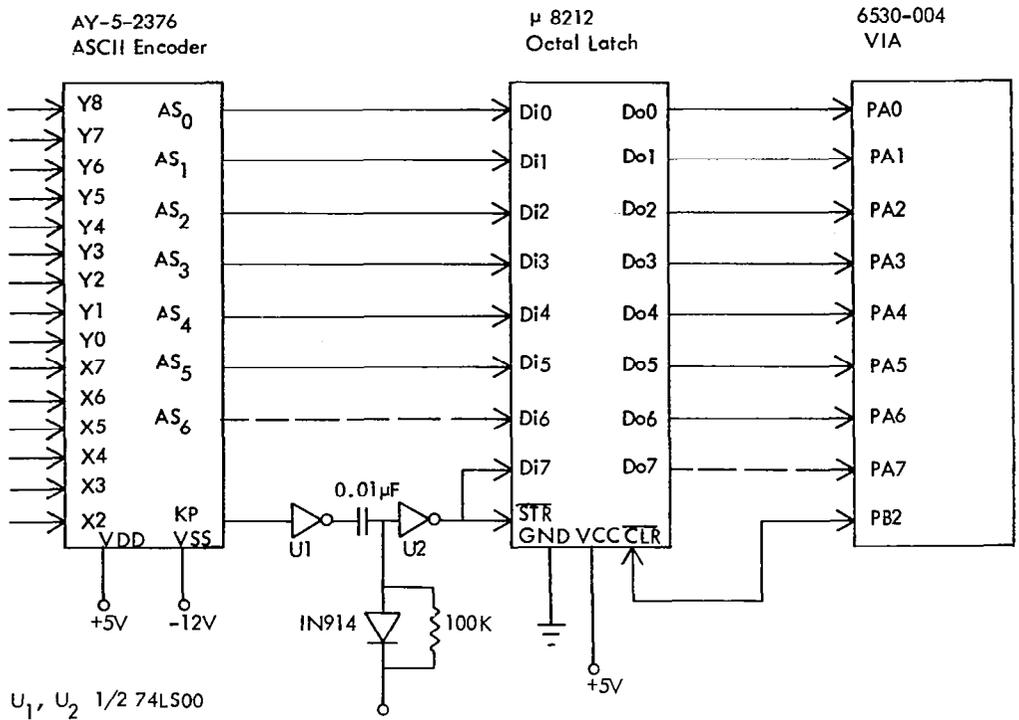
Figure 1. LORAN-C CONTROL/DISPLAY

7	8	9
4	5	6
1	2	3
.	0	D
B S P	E N T	S K I P
C N C L	S C	N A V
P W R	S W	A W

Figure 2. Proposed ASCII Keypad Layout.

		CONNECT →		TO OBTAIN ↓		X ₀	X ₁	X ₂	X ₃	X ₄	X ₅	X ₆	X ₇
Y ₀	NORMAL	NUL	DLE	-	B	;	l	o	9				
	SHIFT	NUL	DLE	"	NUL	+	L	0)				
	CONTROL	NUL	DLE	NUL	NUL	NUL	FF	SI	NUL				
Y ₁	NORMAL	SOH	K	FS	:	/	k	i	8				
	SHIFT	SOH	□	FS	*	?	K	I	(
	CONTROL	SOH	VT	FS	NUL	NUL	VT	HT	NUL				
Y ₂	NORMAL	STX	L	GS	p	.	j	u	7				
	SHIFT	STX	\	GS	P	>	J	U	'				
	CONTROL	STX	FF	GS	DLE	NUL	LF	NAK	NUL				
Y ₃	NORMAL	ETX	N	RS	—	,	h	y	6				
	SHIFT	ETX	^	RS	DEL	<	H	Y	8				
	CONTROL	ETX	SO	RS	US	NUL	BS	EM	NUL				
Y ₄	NORMAL	EOT	M	US	e	m	g	c	5				
	SHIFT	EOT	□	US	'	M	G	T	%				
	CONTROL	EOT	CR	US	NUL	CR	BEL	DC ₄	NUL				
Y ₅	NORMAL	ENQ	NAK	<	BS	n	f	r	4				
	SHIFT	ENQ	NAK	<	BS	N	F	R	\$				
	CONTROL	ENQ	NAK	NUL	BS	SO	ACK	DC ₂	NUL				
Y ₆	NORMAL	ACK	SYN	>	□	b	d	e	3				
	SHIFT	ACK	SYN	>	□	B	D	E	/				
	CONTROL	ACK	SYN	NUL	ESC	STX	EOT	ENQ	NUL				
Y ₇	NORMAL	BEL	ETB	,	□	v	s	w	2				
	SHIFT	BEL	ETB	,	□	V	S	W	"				
	CONTROL	BEL	ETB	NUL	GS	SYN	DC ₃	ETB	NUL				
Y ₈	NORMAL	DC1	CAN	SP	CR	c	a	a	1				
	SHIFT	DC1	CAN	SP	CR	C	A	Q	!				
	CONTROL	DC1	CAN	SP	CR	ETX	SOH	DC1	NUL				
Y ₉	NORMAL	P	EM	.	LF	x	FF	HT	^				
	SHIFT	e	EM	.	LF	X	FF	HT	~				
	CONTROL	DLE	EM	NUL	LF	CAN	FF	HT	RS				
Y ₁₀	NORMAL	O	SUB	—	DEL	z	ESC	VT	\				
	SHIFT	—	SUB	—	DEL	Z	ESC	VT	:				
	CONTROL	SI	SUB	US	DEL	SUB	ESC	VT	FS				

Figure 3. Code Assignment Chart - AY-5-2376 Keyboard Encoder



U₁, U₂ 1/2 74LS00

Figure 4. ASCII Keyboard Encoder Using AY-5-2376.

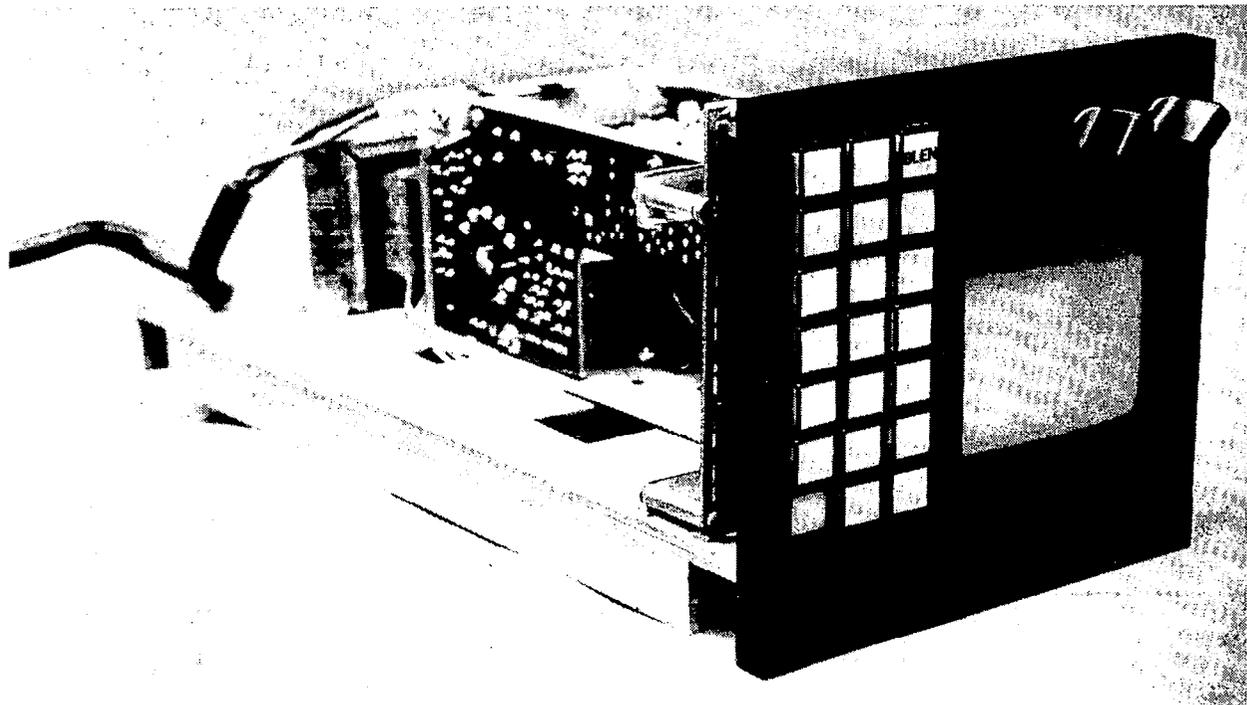


Figure 5. Proposed Display Unit.

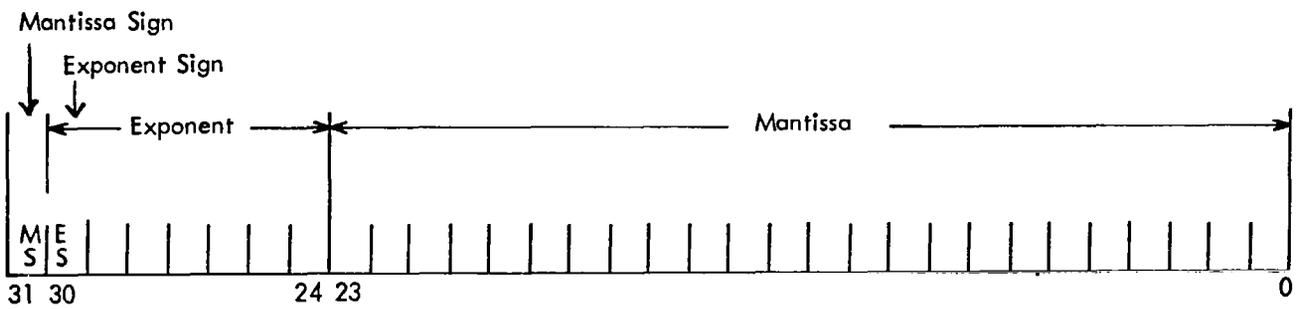


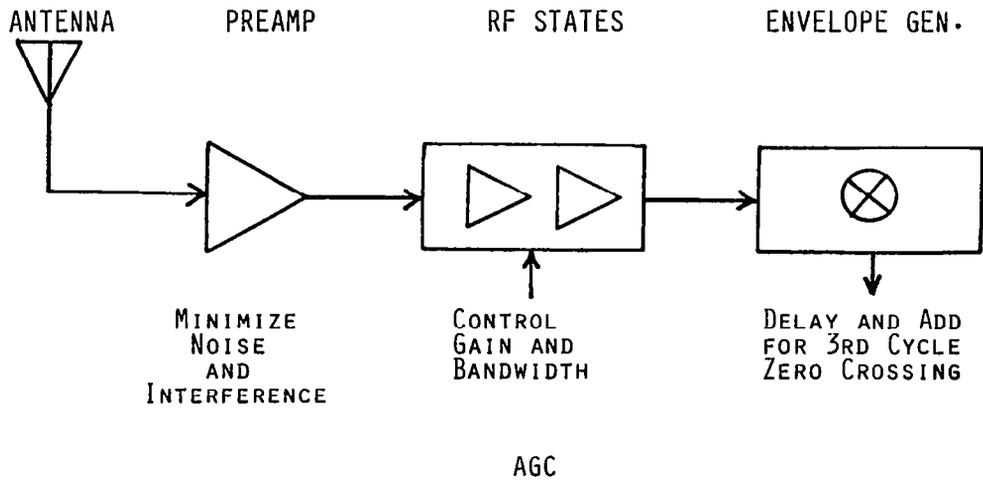
Figure 6. AM9511A 32-Bit Floating-Point Format.

R. F. PROCESSING

Ralph W. Burhans

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Department of Electrical Engineering
Ohio University
Athens, Ohio 45701

LORAN-C RF PROCESSING



INTERFACE TO MICROPROCESSOR

RF SPECTRUM DATA

WEAK VLF SIGNALS

GBR 50 Hz SHIFT

PULSE SIGNALS

ADAPTER FOR STANDARD

COM RECEIVER

LORAN-C RESULTS

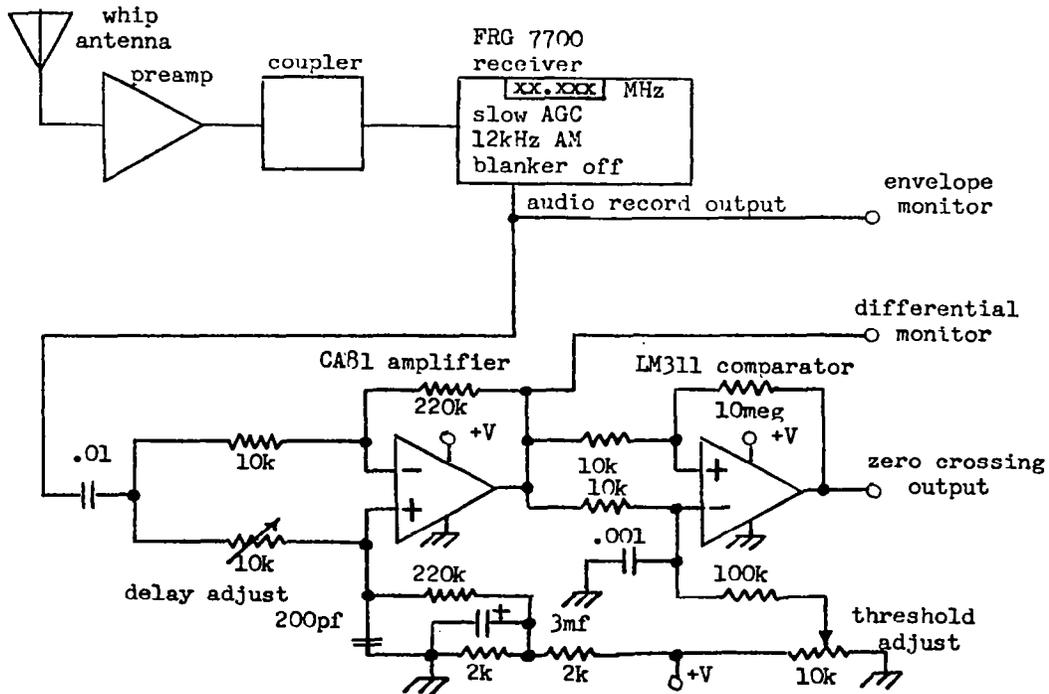
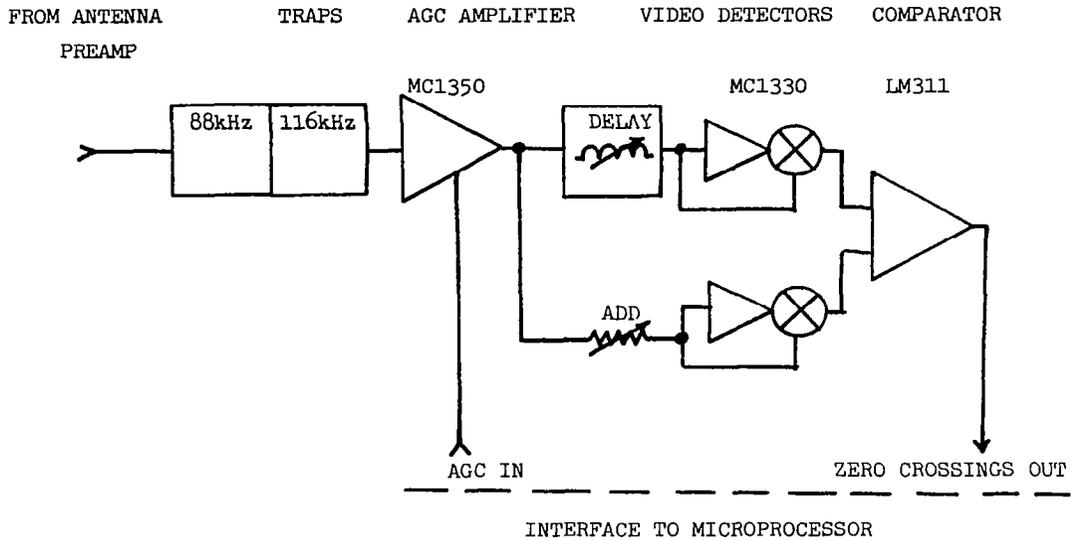
HF RADAR RESULTS

IONOSPHERE SCATTER FROM DISCOVERER II LAUNCH

"WOODPECKER" CHARACTER

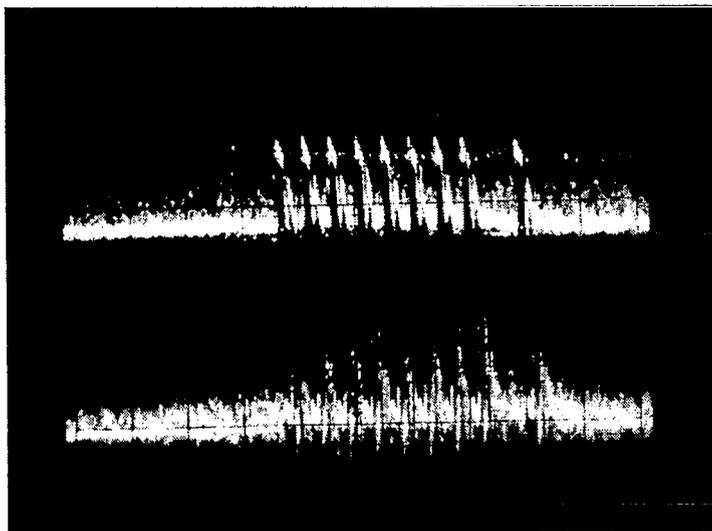
LORAN-C RF PROCESSOR

PROPOSED 1982 DESIGN

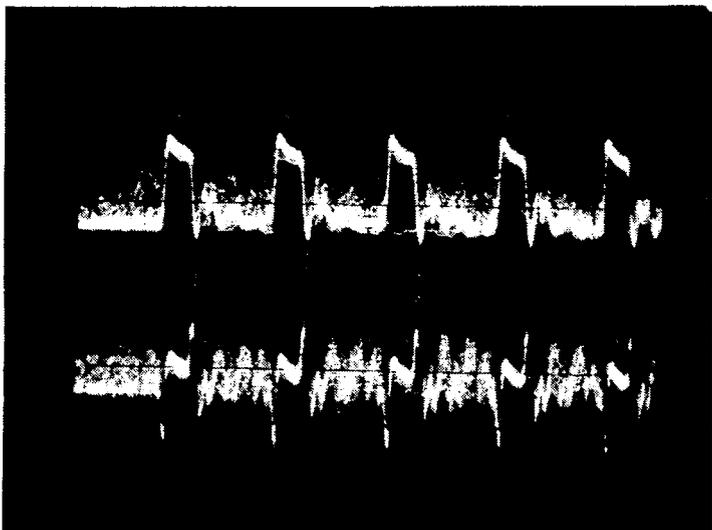


AUGMENTED DIFFERENTIATOR FOR PULSE ENVELOPES

Circuit adapts conventional communications receiver with wideband AM capability to detection of pulse signals such as Loran-C. Also enhances reception for surveillance and observation of HF over-the-horizon radar signals or others where time difference estimates between pulse returns are of interest.



SWEEP 2.0ms/division
 TOP Direct Receiver Envelope
 BOTTOM Differentiated Envelope

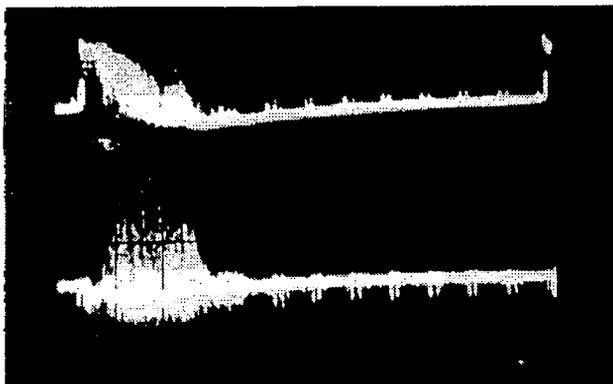


SWEEP 0.5ms/division
 TOP Direct Receiver Envelope
 BOTTOM Differentiated Envelope

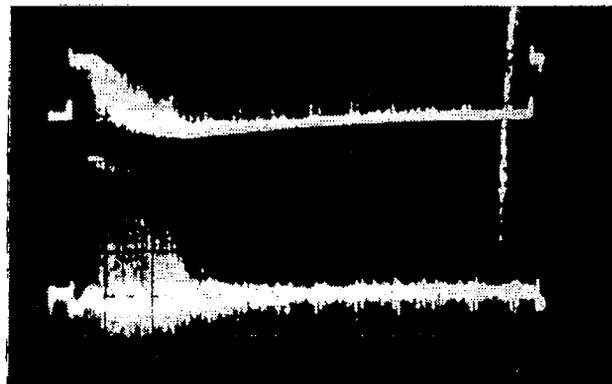
20:00 EST 11/4/81 SENECA, N.Y., MASTER ON 99600 μ sec. GRI

DIFFERENTIAL LORAN-C ENVELOPE SIGNALS

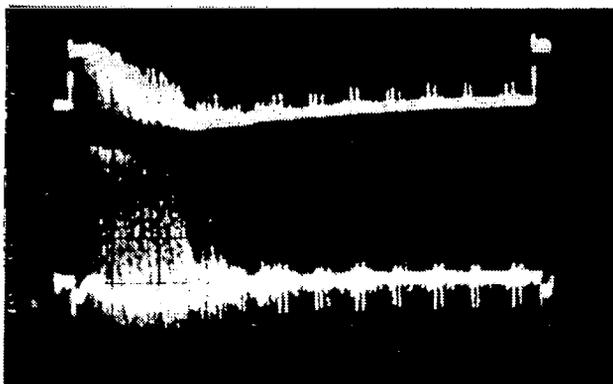
As observed with YAESU FRG 7700 Communications Receiver, 12 kHz bandwidth, slow AGC, total input signal plus noise level = -66 DBM (20 DB over S9). Signal lag and subtraction circuit provides differential edge or zero crossings from a standard, unmodified communications receiver. Needed for driving external post detection microcomputer or digital tracking system for frequency standard or simple navigation experiments.



10:11AM 26.430MHz 1 minute



10:15AM 26.475MHz 5 minutes



10:17AM 26.430MHz 7 minutes



10:19AM 26.320MHz 9 minutes



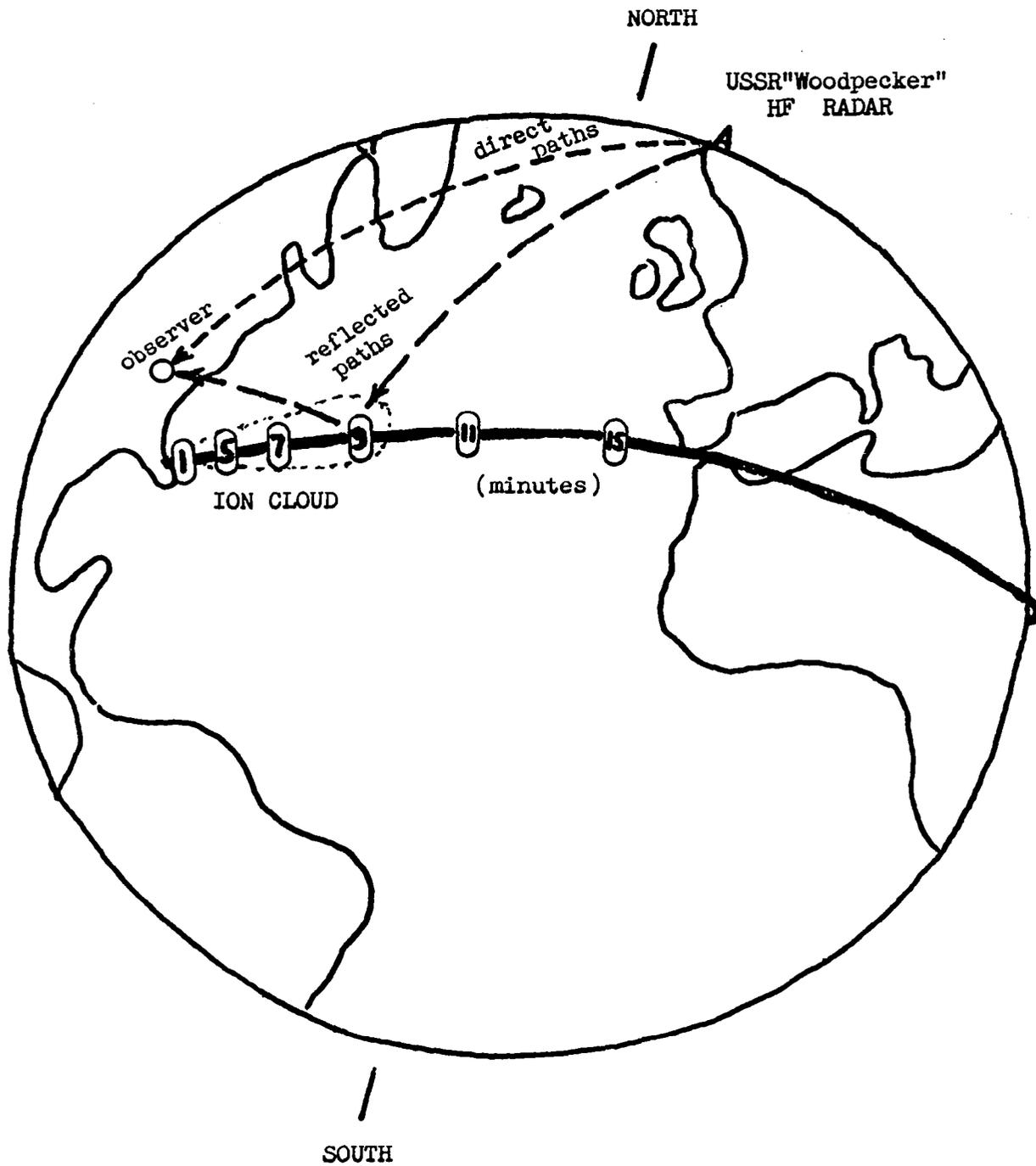
10:21AM 26.320MHz 11 minutes



10:24AM 26.320MHz 14 minutes

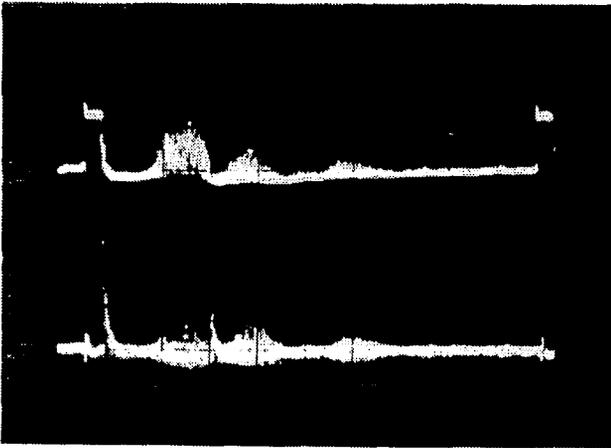
HF OTH RADAR RETURNS AT LAUNCH OF COLUMBIA, SHUTTLE II, November 12, 1981

Top trace is amplitude of received signal. Bottom is differentiated rise time from scattered edges of ionosphere returns. Note, slight increase in amplitude and intensity of scattered returns progressing to 14 minutes after launch. Probable cause is ionized trail from main engine and booster exhaust. The pulse GRI was 100 milliseconds (10ms/division). Variable 120Hz interference present. USSR "Woodpecker" changed channels and direction at about 10:25AM.



APPROXIMATE POSITIONS OF COLUMBIA SHUTTLE AT TIMES OF PHOTOS

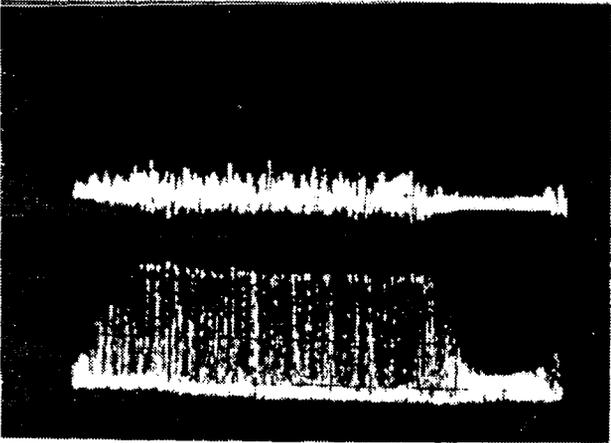
Direct signal path is shorter, arrives at observer before southern ionosphere scatter and much before any rocket exhaust ion enhancement.



22:00 EST 11/4/81
23.800 MHz GRI 100ms , 10ms/div.

4ms main bang with strong secondary scatter at 15-25ms, 27-37ms, and 50-60ms after start of main bang.

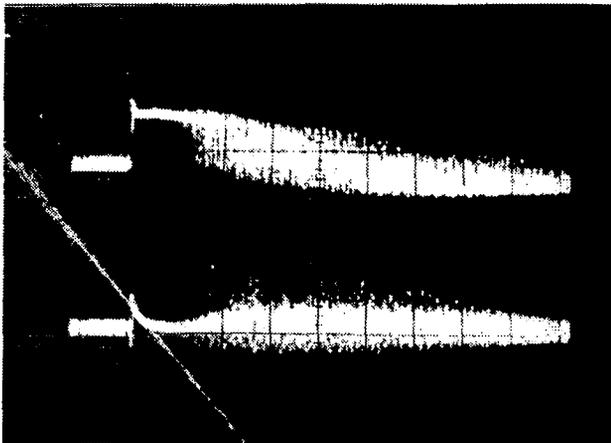
TOP amplitude
BOTTOM DE/DT



09:37 EST 11/2/81
27.900 MHz GRI 100ms , 10ms/div.

Long PN code sequence, no FM

TOP amplitude
BOTTOM DE/DT

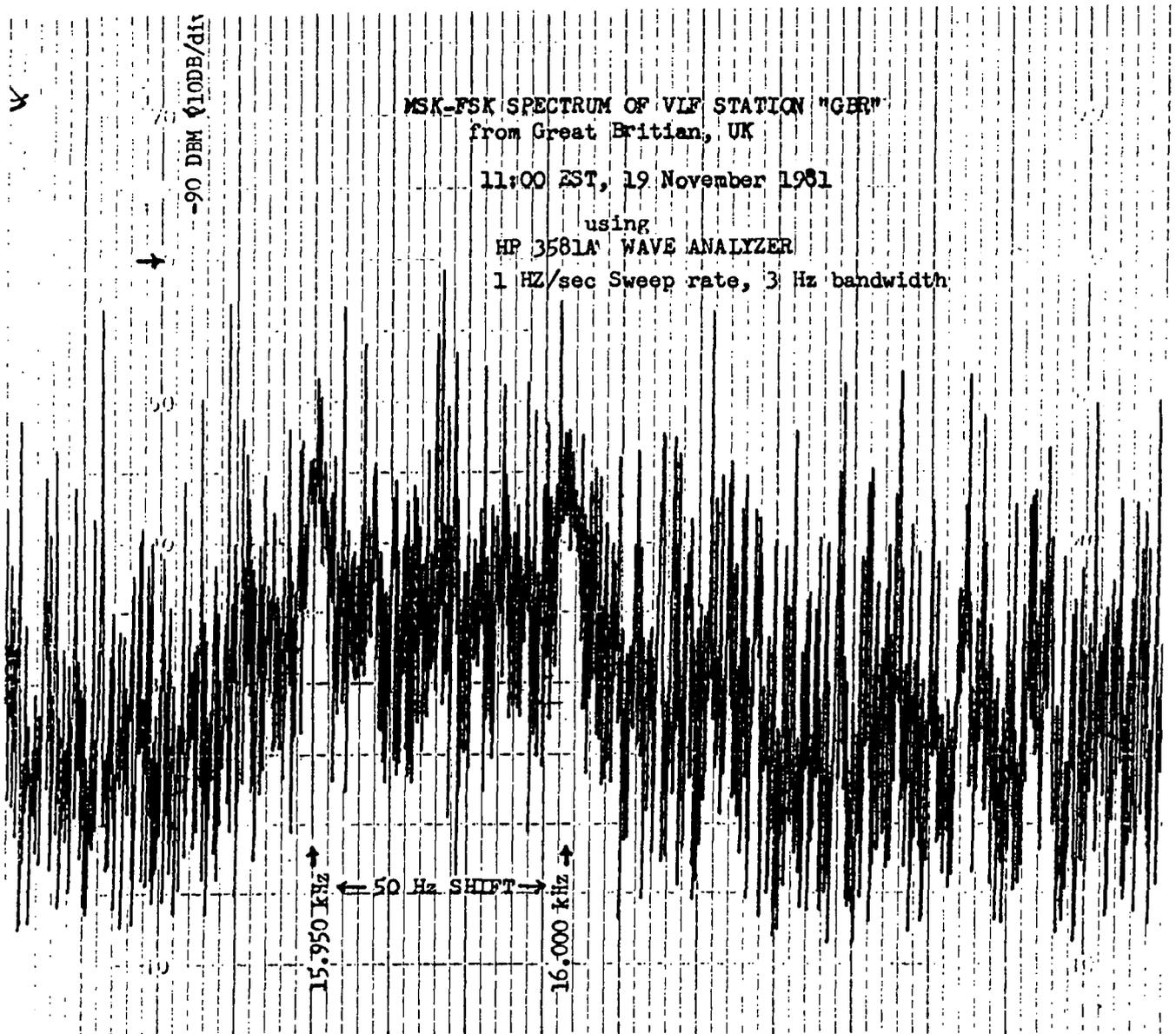


15:37 EST 11/4/81
18.575 MHz GRI 100ms, 4ms/div.

Nominal 4 to 6ms single pulse with much secondary scatter to 36 ms after main bang starts.

TOP amplitude
BOTTOM DE/DT

USSR HF "WOODPECKER" EXAMPLES WITH FRG 7700 RECEIVER



HIGH RESOLUTION VLF SPECTRUM

Example of reception of weak VLF signals using an HP 3581A Wave Analyzer which can detect signals with a very narrow bandwidth of only 3 Hz. The graph shows the 50 Hz frequency shift keying format transmitted by VLF station "GER" on 16 kHz from Rugby, England as received in Athens, Ohio.

PROGRAMMING FOR LORAN-C RECEIVER PILOT DISPLAY

Fujiko Oguri

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Department of Electrical Engineering
Ohio University
Athens, Ohio 45701**

PROGRAMMING FOR LORAN-C RECEIVER PILOT DISPLAY

PROBLEM

Compute: Range, Bearing, Ground Speed, & Cross Track Error
Given: Lat and Long of waypoints and receiver
Using: 6502 CPU and 9511A math chip
For: Final output & pilot display for OU Loran-C Receiver

Earth Model Chosen

Kayton & Fried "Avionics Navigation Systems",
John Wiley & Sons, NY 1969, p. 160.

PROGRESS

Basic equations used check with FORTRAN program for precision.

$$\text{Range} = a\theta - \frac{af}{4} \left[(\sin\beta + \sin\beta_1)^2 \left(\frac{1 - \cos\theta}{\sin\theta} \right) \left(\frac{\theta - \sin\theta}{\sin\theta} \right) + \left(\frac{\sin\beta - \sin\beta_1}{\sin\theta} \right)^2 (1 + \cos\theta)(\theta + \sin\theta) \right]$$

$$(\theta) \text{ Bearing} = \tan^{-1} \left(\frac{\cos\beta_1 \sin(\lambda - \lambda_1)}{\cos\beta \sin\beta_1 - \sin\beta \cos\beta_1 \cos(\lambda - \lambda_1)} \right)$$

where: a = semimajor axis
f = flattening of reference ellipsoid
 ϕ = geodetic latitude of the receiver
 ϕ_1 = geodetic latitude of the waypoint
 $\tan\beta = (1-f)\tan\phi$
 $\tan\beta_1 = (1-f)\tan\phi_1$
 θ = angle from receiver to waypoint
 λ = geodetic longitude of the receiver
 λ_1 = geodetic longitude of the waypoint

PLANNED WORK

Convert to assembly language program for 6502 and 9511 chips

Check precision
anticipate 0.162° mean bearing error
0.0106 nm mean range error

Minimize Time Only 200,000 $\mu\text{sec.}$ (0.2 sec.) available for these computations since lat-long and Loran-C receiver TDs take up remainder of computer time.

After computing range and bearing, other calculations are relatively simple.

PROGRAMMING FOR LORAN-C

COMPUTE RANGE-BEARING-ETC.

FROM LORAN-C DATA

FOR MULTIPLE WAYPOINT POSITIONING

PROGRESS

EQUATIONS EVALUATED

PLANNED EFFORT

CONVERT TO MACHINE LANGUAGE

CHECK ACCURACY

MINIMIZE COMPUTER TIME

COMPREHENSIVE INVESTIGATION OF LORAN-C

FOR GA APPLICATION

Stephen R. Yost

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Ohio University
Athens, Ohio 45701

COMPREHENSIVE INVESTIGATION OF LORAN-C FOR GA APPLICATION

- I. ESTABLISH PERFORMANCE CRITERIA
 - A) FAA ENROUTE, TERMINAL, AND APPROACH ACCURACY REQUIREMENTS
 - B) SUMMARIZE PREVIOUSLY COLLECTED O.U. LORAN-C DATA
- II. DATA ANALYSIS TECHNIQUES
 - A) INFORMATION SEARCH TO DETERMINE THE MOST CONCLUSIVE METHODS FOR STATISTICAL ANALYSIS
 - 1) DETERMINE OPTIMUM SIZE OF A STATISTICAL SAMPLE
 - B) MULTIPLE, SIMULTANEOUS LORAN-C RECEIVER DATA COLLECTION
 - 1) UTILIZATION OF CASSETTE TAPE DATA RECORDERS
 - C) USE OF OHIO U COMPUTER SYSTEM FOR DATA REDUCTION AND ANALYSIS
- III. GROUND MONITORING
 - A) LONG-TERM ON-SITE MONITORING OF LORAN-C POSITIONAL DATA
 - 1) EXAMINE DAILY AND POSSIBLY SEASONAL LORAN-C COVERAGE GRID WARPAGE
 - 2) DETERMINE LORAN-C WAYPOINT VALUES FOR RUNWAY THRESHOLDS
 - B) SELECTION OF TEST SITES
 - 1) AREAS WHICH ARE COVERED BY MORE THAN ONE LORAN-C CHAIN PERMITTING CROSS-CHAIN POSITION COMPARISON
 - 2) EXAMINE LORAN-C PERFORMANCE IN FRINGE COVERAGE AREAS
- IV. FLIGHT TESTING
 - A) USE OF AN ABSOLUTE DATA REFERENCE TO SUBSTANTIATE LORAN-C DATA
 - B) SIMULATE APPROACHES USING PREVIOUSLY DEFINED LORAN-C WAYPOINTS
 - C) EXAMINE THE EFFECTS OF NON-GEOGRAPHIC IRREGULARITIES ON LORAN-C FLIGHT PATH DATA
- V. CONCLUSIONS
 - A) FORMULATE SPECIFIC HARDWARE AND SOFTWARE IMPROVEMENTS TO TO THE OHIO U LORAN-C RECEIVER
 - B) COLLECTIVELY EXAMINE THE EFFECTS OF OVERLAND PROPAGATION DELAY TO LORAN-C SIGNALS
 - C) ADDRESS THE POSSIBLE INTEGRATION OF LORAN-C NAVIGATION TO CURRENT ATC SYSTEM

**Princeton
University**

INVESTIGATION OF AIR TRANSPORTATION TECHNOLOGY
AT PRINCETON UNIVERSITY, 1981

Professor Robert F. Stengel
Department of Mechanical and Aerospace Engineering
Princeton University
Princeton, New Jersey 08544

SUMMARY OF RESEARCH

The Air Transportation Technology Program at Princeton University, a program emphasizing graduate and undergraduate student research, proceeded along seven avenues during the past year:

- Investigation of Fuel-Use Characteristics of General Aviation Aircraft
- Investigation of a Dead-Reckoning Concept Incorporating a Fluidic Rate Sensor
- Experimentation with an Ultrasonic Altimeter
- Development of Laser-Based Collision Avoidance Systems
- Flight Path Reconstruction from Sequential DME Data
- Application of Fiber Optics in Flight Control Systems
- Voice Recognition Inputs for Navigation/Communication Receiver Tuning

Principal investigators Robert Stengel and Larry Sweet have worked with Prof. H.C. Curtiss and Richard Miles in advising the students participating in this program.

Navigation research conducted during earlier years provided a logical stepping stone to consideration of flight management systems for general aviation aircraft, including fuel-minimizing guidance between origin and destination points. The effectiveness of such guidance logic is, of course, dependent on the accuracy of aircraft fuel-use models, and this, in turn, requires adequate mathematical description of engine characteristics. In his doctoral research, Richard Parkinson has developed a cruise performance model that can be developed from operating handbook data, and he has developed a detailed mathematical model of the fuel-use characteristics of general aviation reciprocating engines. Interim results are documented in a technical paper{1}, and his thesis is near completion. Mr. Parkinson began his research under the guidance of Prof. Dunstan Graham, who retired from the university in 1980; he has continued with the supervision of Prof. Curtiss and Sweet. Graduate student Eugene Morelli is continuing this research.

A simple approach for dead reckoning navigation that is enhanced by the use of a fluidic angular rate sensor has been studied by M.S.E. candidate Robert Ellis. The fluidic sensor is used to correct the northerly turning error of conventional flux gate magnetic compasses. (The northerly turning error results from the effect of "dip angle" on sensed magnetic heading when the aircraft is banked to turn.) Limited flight tests were conducted during the year, and final results of experimental studies will be reported in Mr. Ellis's thesis. Mr. Ellis began his research with former principal investigator Dunstan Graham; Prof. Sweet is his current advisor.

Amy Snyder, a junior in mechanical and aerospace engineering, completed an investigation of the feasibility of using an ultrasonic transducer as an altimeter for the landing approach through touchdown. The transducer, initially developed for use in an automatic range-finding camera, demonstrated better than 1% accuracy for ranges of 0.27 to 10.67 m (0.9 to 35 ft) in laboratory and wind tunnel tests, with transverse air velocities of up to 45.7 m/sec (150 ft/sec) and with sensor angles of 0 to 25 deg². Senior Philip Chu is continuing this research, with the objectives of doubling the sensor's range and conducting flight tests of the system. Prof. Stengel has been Ms. Snyder's and Mr. Chu's advisor.

The investigation of laser-based collision avoidance systems continued, resulting in several papers, reports, and theses^{3-8}. This research is being conducted in parallel with a NASA Ames-sponsored study of short-range tracking between two cooperative aircraft using low-power lasers. Demonstration equipment has been assembled and will be tested in flight within the near future. This research has involved Prof. Richard Miles and Larry Sweet, graduate students Steven Webb, Edward Wong, and Gregory Russell, and undergraduates Leonard Blackburn and Maged Tomeh.

The Flight Research Laboratory is engaged in a continuing study of flying qualities criteria for single-pilot instrument flight operations with separate sponsorship from NASA Langley Research Center^{9}, and elements of the flight path reconstruction algorithms, which have common application for the study of air transportation technology, have been developed under this grant. Techniques for applying extended-optimal smoothing to sequential DME data and on-board inertial and air data have been developed and applied to flight test data by Ph.D. candidate Aharon Bar-Gill. In this approach, a single DME receiver is switched between alternate DME stations to update the state estimate, which is processed after the flight has been completed. Because all the measured data are applied to estimate the state at each point in the flight path, the result is somewhat more accurate than that which would be obtained from the extended-optimal filter. Mr. Bar-Gill is advised by Prof. Stengel.

Fiber optic data transmission promises to provide decreased weight, improved resistance to electro-magnetic interference, and increased reliability in future active flight control systems. Graduate student Kristin Farry is nearing completion of an application of fiber-optic technology in a multi-microprocessor system, with the combined sponsorship of this grant and the Office of Naval Research. Princeton's Variable-Response Research Aircraft (VRA) has dual angle-of-attack and sideslip angle vanes mounted at each wingtip, previously connected to the central analog and digital control logic by standard wiring. Dual microprocessors have been installed at the wingtips; the sensors are connected directly to these units, which in turn communicate with the central microprocessor via fiber-optic links. The local processors provide scaling and instrument-error correction, elimination of roll rate effects on sensed angles, and analog/digital conversion before sending the data to the flight control computer unit. The fiber-optic multiprocessor system will be tested in flight shortly, and the results will be presented in Ms. Farry's M.S.E. thesis. Ms. Farry is working with the guidance of Prof. Stengel.

Voice recognition of pilot inputs could play a major role in future air transportation, not only for commercial aircraft but for general aviation aircraft as well. This capability has particular significance for single-pilot instrument-flight operations, where one pilot is required to perform all the tasks normally carried out by two or three persons in the larger aircraft. The tasks that could be carried out using voice command are varied; as a generality, these are characterized as the jobs which a captain might ask the co-pilot to do, e.g., tuning radios, maintaining contact with air traffic control, holding altitude, and so on. Frances Koo, a senior in electrical engineering and computer science, is conducting a project in which voice recognition will be used to tune the navigation and communication receivers in Princeton's Avionics Research Aircraft (ARA). The ARA's receivers will be tuned by digital signals from a microprocessor, which will receive inputs from the pilot via the voice recognition board. Ms. Koo is being advised by Prof. Stengel.

In addition, the research on OMEGA-Dead Reckoning hybrid navigation completed earlier has been documented in the M.S.E. thesis of Ralph Nichols{10}, completed this year. Mr. Nichols began his research under the guidance of Prof. Graham and completed his thesis with Prof. Stengel as his advisor.

The NASA grant supporting student research in air transportation technology has inestimable value in helping educate a new generation of engineers for the aerospace industry, and it is producing research results that are relevant to the continued excellence of aeronautical development in this country.

REFERENCES AND ANNOTATED BIBLIOGRAPHY

1. R.C.H. Parkinson, "An Operational Model of Specific Range for Microprocessor Applications in Piston-Prop General Aviation Airplanes", AIAA Paper No. 81-2330, Nov 1981.

The paper describes a cruise performance model for conventional general aviation airplanes of fixed design, powered by naturally aspirated spark ignition piston engines and constant-speed propellers. The model computes the airplane operating point which maximizes specific range and is suitable for airborne microprocessor implementation, with the assumptions that the engine ignition timing is optimized for maximum engine torque and that fuel-air mass ratio can be controlled. It appears that fuel savings of 20% to 26% could be achieved through use of this procedure.

2. Amy V. Snyder, "Ultrasonic Altimetry: Feasibility and Design Principles", Princeton M.A.E. Junior Independent Research Project Report, Princeton University, May 1981.

The report examines the feasibility of using a Polaroid Ultrasonic Ranging System as an altimeter for aircraft on landing approach. The ranging device generates pulses in the 50 to 60 KHz band using an electrostatic transducer that functions as both an emitter and a receiver of the sound energy. Initial wind tunnel tests indicated that the flow of air over the unshielded transducer generated sounds in the operating band that precluded ranging; however, a megaphone-like baffle was found to restore ranging capability with air velocities up to 45.7 m/sec (150 ft/sec). This technique shows great promise for providing landing approach data at low cost, with high reliability, and for aircraft of all classes.

3. Richard B. Miles, "Laser Beacon System for Aircraft Collision Hazard Determination", Applied Optics, Vol. 19, No. 13, July 1, 1980, pp. 2098-2108.

A laser beacon collision hazard determination system is capable of simultaneously determining range, bearing, and heading of threat aircraft. Calculations demonstrate that threat aircraft may be observed at >10 km under good visibility conditions, the conditions under which the overwhelming majority of mid-air collisions take place. A wide variety of detection systems may be chosen based on cost, detection range, and sophistication. Preliminary tests demonstrate that accurate range measurements are possible under daylight conditions.

4. Leonard A. Blackburn II, "A Display for a Laser Aircraft Position Locator System", Princeton M.A.E. Senior Independent Research Project Report, Princeton University, May 1981.

The purpose of this study was to develop a system that displays the relative (three-axis) position between a research aircraft and a following helicopter. Signals would be displayed in such a way that the helicopter pilot could hold position relative to the other aircraft to within one foot in distance and one degree in azimuth and elevation angles. The study included the selection and construction of a data acquisition system, the design of a suitable display, and the analysis of position control and pilot-helicopter dynamics using root-locus techniques. Helicopter dynamics were simulated using an eleventh-order, six-degree-of-freedom model; the pilot was modelled by a conventional compensatory transfer function. Particular attention was paid to the pilot gains and lead-lag compensation required for closed-loop stability. The analysis indicated that stabilizing the system would require substantial pilot effort at the data sampling intervals anticipated.

5. Maged Tomeh, "Non-Linear State Estimation Algorithms for the Development of an Air-Collision Avoidance System Using Laser Beacons", Princeton M.A.E. Senior Independent Research Project Report, Princeton University, May 1981.

An extended Kalman filtering algorithm based on a nonlinear dynamic system model was applied to the collision avoidance problem. The purpose was to assess the level of estimation accuracy that could be obtained in determining the flight path of threat aircraft and to evaluate on-board implementation using steady-state filter gains. Over 50 simulations of near-collision flight paths were computed. The filter was found to possess extreme sensitivity to initial conditions and an inherent instability in estimating one of the unmeasured state variables. Suggestions for improving the filter's characteristics centered on the use of a discrete linear Kalman filter.

6. Steven G. Webb, "Aircraft Position Measurement Using Laser Beacon Optics", Princeton M.S.E. Thesis, M.A.E. Report No. 1535-T, Princeton University, Sept. 1981.

The thesis investigates a system to precisely measure the relative position between two aircraft utilizing a laser beacon, an optical detector array, and on-board digital computation. The laser beacon consists of two orthogonal fan-shaped narrow-width beams with 166-deg coverage, each rotating at four revolutions per second. Each of the four detectors in the receiving array is composed of two compound parabolic concentrators which collect the incoming laser beams over a 150-deg field of view, collimate the light so that it can pass through an interference filter, and concentrate the beam on a photodiode. The diode converts the detected beams to pulses that are transmitted through a bandpass filter and processed for tracking purposes. Initial tests have demonstrated the system's potential for use as a position measuring system.

7. L.M. Sweet, R.B. Miles, S.G. Webb, and E.Y. Wong, "Wide Field of View Laser Beacon System for Three-Dimensional Aircraft Position Measurement", ASME Paper No. 81-WA/DSC-9, Nov 1981.

This paper describes a new wide-field-of-view laser beacon system for measurement, in three dimensions, of aircraft or other remote objects. The system provides aircraft collision hazard warning independent of ground-based hardware, and it has applications in flight research, helicopter-assisted construction and rescue, and robotic manipulation. Accurate information describing the relative range, elevation, and azimuth of the aircraft is generated by the sweep of a low-power fan-shaped rotating laser beacon past an array of optical detectors. System reliability and performance are enhanced through bandpass filtering of the pulse signals, digital logic designed to mask spurious signals, and adaptive modulation of trigger threshold levels.

8. L.M. Sweet, R.B. Miles, G.F. Russell, M.G. Tomeh, S.G. Webb, and E.Y. Wong, "Digital Detection and Processing of Laser Beacon Signals for Aircraft Collision Hazard Warning", AIAA Paper No. 81-2328, Nov 1981.

A low-cost collision hazard warning system suitable for implementation in both general and commercial aviation is presented. The laser beacon/photodetector system provides direct measurement of relative aircraft positions, using optimal nonlinear estimation theory. The measurements resulting from the current beacon sweep are combined with previous data to provide the best estimate of aircraft proximity, heading, minimum passing distance, and time to closest approach.

9. A. Bar-Gill, W.B. Nixon, and G.E. Miller, "Flying Qualities Criteria for Single-Pilot Instrument Flight Operations", Princeton M.A.E. Report No. 1528, Dec 1981.

Preparations for flight test related to the development of flying qualities criteria for Single-Pilot Instrument Flight Rule (SPIFR) operations are described. The principal objective is to examine the effects of aircraft dynamic characteristics (representative of long period stability and ease of longitudinal trim variations) on pilot opinion, pilot workload, and flight technical error during simulated IFR missions in general aviation aircraft. The Avionics Research Aircraft (ARA) has been modified and adapted for SPIFR operations. Aircraft configurations to be tested using the ARA's variable-stability fly-by-wire system have been chosen and matched in flight. The mission matrix has been designed. Microprocessor software for the on-board data acquisition system has been flight tested. Flight path reconstruction procedures are in a final stage of computer program

development. Work has begun on algorithms associated with the statistical analysis of flight test results.

10. Ralph A. Nichols, Jr., "Implementation and Evaluation of an OMEGA-Dead Reckoning Hybrid Navigation System", Princeton M.S.E. Thesis, M.A.E. Report No. 1523-T, Princeton University, June 1981.

This thesis reports on the results of flight tests in which navigation is accomplished by combining data from an OMEGA radio receiver with heading and true air speed measurements. The implementation and evaluation of the system, which was installed in Princeton's LASA 60 utility aircraft, are discussed, including fabrication, hardware configuration, and software design. Flight test procedures are described, the theoretical basis for analysis is developed, and flight test results are presented. These flight tests showed 10% to 40% reductions in rms position errors over that obtained from OMEGA data alone. Raw OMEGA position errors typically ranged from 0.8 to 1.8 nm (rms). OMEGA signals were found to contain large amplitude, low frequency noise; flight test results were consistent with pre-flight predictions for noise of this type. The hybrid system improved navigation continuity with poor OMEGA signal reception. OMEGA lane count could be maintained during as much as an hour of signal loss. It was concluded that OMEGA navigation does not provide sufficient accuracy for general aviation operations over the continental United States, although improvements could be made in the navigation algorithm.



FLYING QUALITIES CRITERIA FOR GA
SINGLE PILOT IFR OPERATIONS

AHARON BAR-GILL
PRINCETON UNIVERSITY

BACKGROUND

- o Over 200,000 GA aircraft operational in U.S. only
- o Over 40,000,000 flight hours per year

PROBLEM

GA accident statistics investigated by NASA (TM 78773) and attributed mostly to the SPIFR flight regime - due to coupling of the following effects:

- o Low frequency aircraft dynamics deficiencies (no design criteria in FAR #23,181, wind shear)
- o High workload environment
- o IFR pilot experience
- o Limited GA instrumentation (compared to airliners, e.g.)

DIRECTIONS FOR SOLUTION

- o Autopilots (wing levelers, etc., e.g., NASA CP 2170)
- o Training (GA simulators, including IFR conditions, become available; e.g., Aviation Week and Space Tech., 11/30/81)
- o Instrumentation improvements (advanced displays, DME sequencing, Loran C, etc.)
- o Aircraft low frequency dynamic response improvement - to date little has been done in this area

MEANS

- o Theoretical work
- o Ground simulators - done a lot
- o Actual flight testing plus extensive statistical analysis - much less

Modern control theory algorithms are employed to identify the most important - in the SPIFR context - aerodynamic configurations and to implement these configurations on the test vehicle.

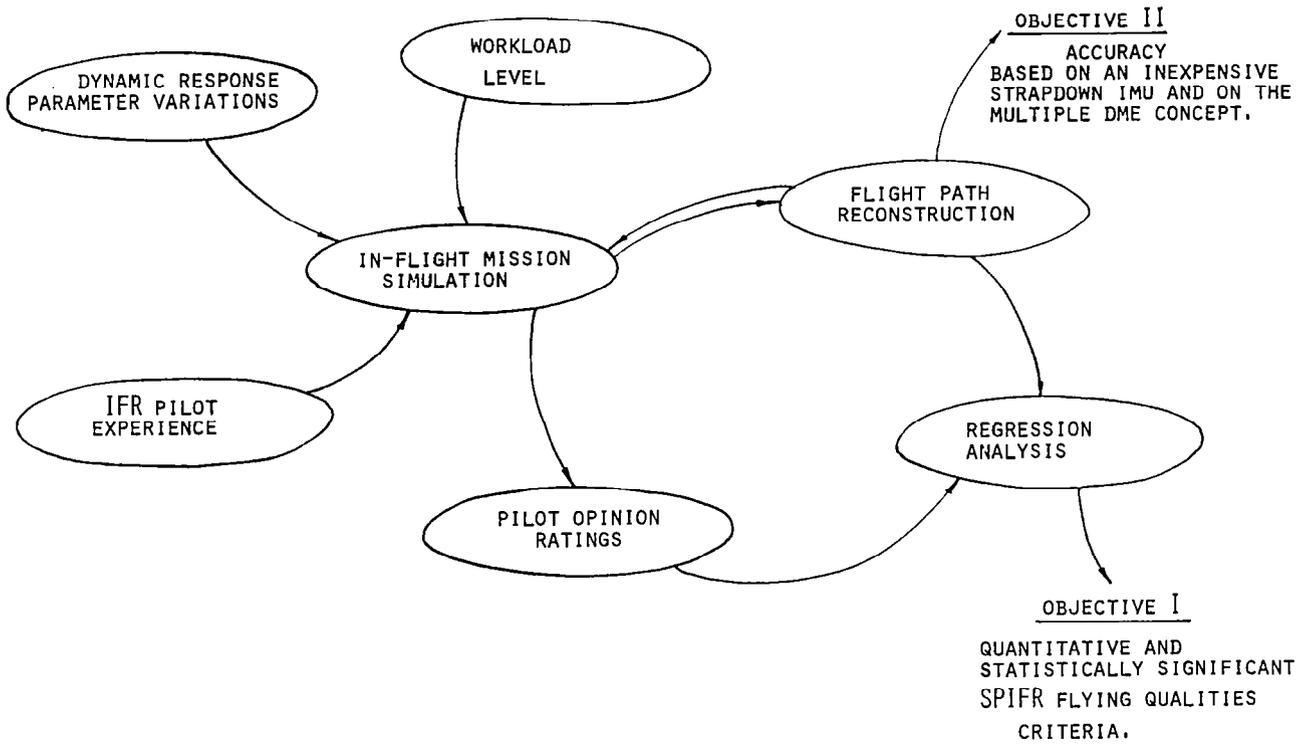
The experimental vehicle is the Ryan Navion, which has been modified and instrumented to a level of a fly-by-wire system, capable of in-flight simulating a wide range of aerodynamic configurations.

The sensor package includes a strapdown IMU, and airspeed, altitude, and aerodynamic angles sensors. The navigational package provides VOR/DME measurements. Control manipulation time histories are recorded as well.

SPIFR RESEARCH - FRL, PRINCETON

- o IDENTIFICATION OF KEY AERODYNAMIC CONFIGURATIONS
- o IMPLEMENTATION ON THE ARA IN-FLIGHT SIMULATOR
- o MISSION MATRIX DESIGN
- o EXPERIMENTAL SYSTEM
- o DATA REDUCTION
- o OPTIMAL FLIGHT PATH RECONSTRUCTION
- o REPRESENTATIVE RESULTS

LOGICAL FLOW CHART OF THE SPIFR RESEARCH



Formulation of the output command algorithm has been presented by Professor R. F. Stengel at the TRI-UNIV Conference in Boston, September 1980, and is discussed in the context of the SPIFR research in a report entitled Flying Qualities Criteria for Single-Pilot Instrument Flight Operations (M.A.E. Report No. 1528, Princeton University, December 1981). Implementation of the implicit model following algorithms may also be found in this report.

Ranges of variation in the aerodynamic parameters are intended to reflect possible trends in GA aircraft design.

IDENTIFICATION OF HIGHER-PRIORITY AERODYNAMIC CONFIGURATIONS

- O OUTPUT COMMAND ALGORITHM
- O COMPLETE DYNAMIC SIMULATION

CRITERIA FOR REPRESENTATION OF CHOSEN CONFIGURATIONS

- O INPUT AND OUTPUT STEADY STATES
- O TRANSIENT RESPONSE CHARACTERISTICS

IMPLEMENTATION OF CHOSEN CONFIGURATIONS ON ARA IN-FLIGHT SIMULATOR

- O IMPLICIT MODEL FOLLOWING ALGORITHM

The experimental matrix is designed to provide a range of low-frequency aircraft flight characteristics. The numbers indicate how many replications will be made for each configuration and test subject. The pluses and minuses indicate whether the parameter variation will be positive or negative.

EXPERIMENTAL MATRIX DESIGN

TRADEOFF BETWEEN

- NUMBER OF CONFIGURATIONS,
- NUMBER OF REPLICATIONS,
- NUMBER OF EVALUATION PILOTS

(UNDER THE CONSTRAINT OF ~ 30 FLIGHT HOURS)

CONFIGURATION	PRINCETON TEST PILOT	NASA PILOT	GA PILOT	NO. OF MISSION RUNS
NOM.	2	2	2	6
X_U	2 \pm	2 \pm	3 $\pm\pm$	7
Z_U	2 \pm	2 \pm	4 $\pm\pm$	8
Z_W	2 \pm	2 \pm	3 \pm	7
M_U	2 \pm	2 \pm	4 $\pm\pm$	8
$M_{\delta T}$	3 \pm	3 \pm	4 $\pm\pm$	10
$Z_{\delta E}$	2 \pm	2 \pm	4 $\pm\pm$	8
$Z_{\delta T}$	2 \pm	2 \pm	4 $\pm\pm$	8

$$\Sigma = 62$$

FLIGHT PLAN FOR EACH PILOT IS OF FOLLOWING STRUCTURE:

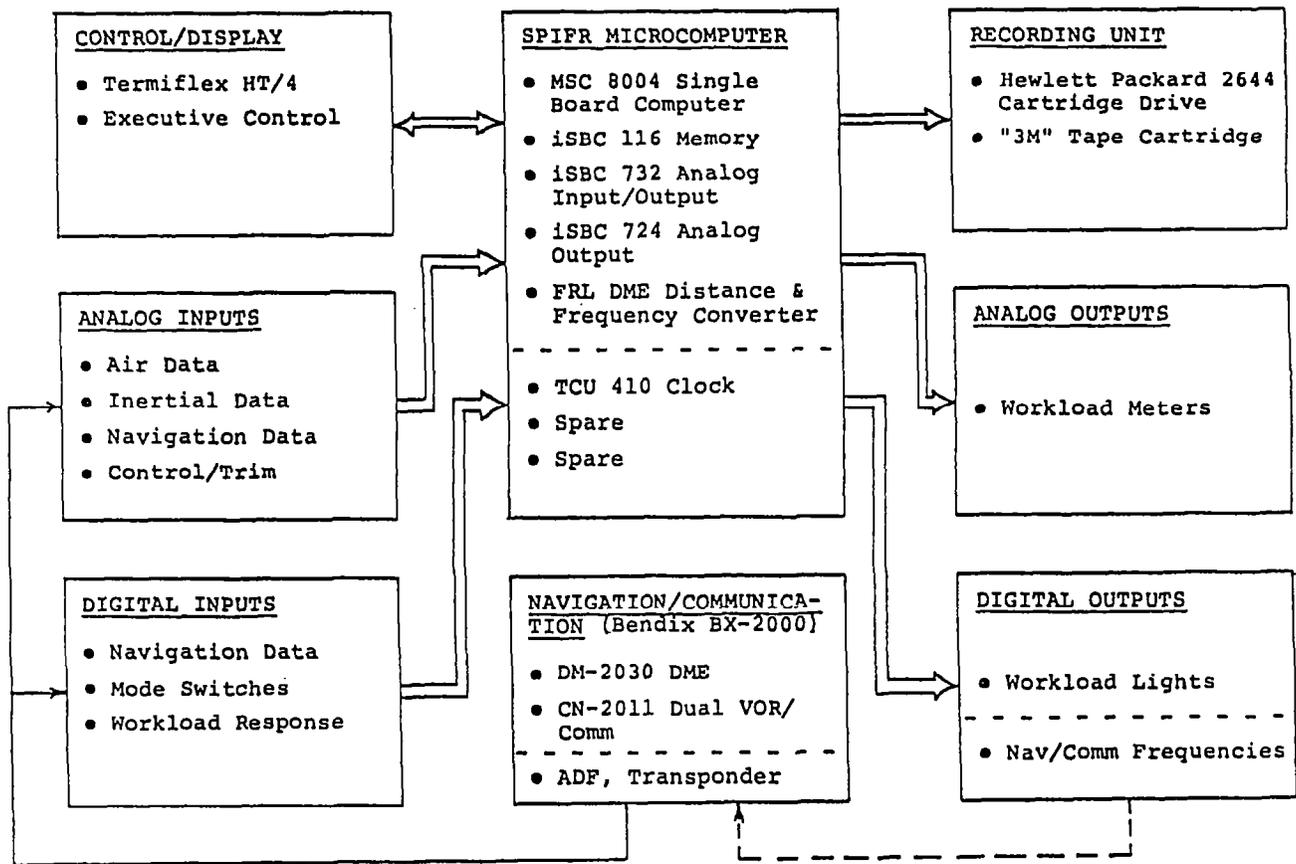
TAKEOFF NO.	MISSION NO.	CONFIGURATION NO.	TRACK NO.
1	1	1 (NOM)	1
	2	2	2
	3	6	3
2	4	1	2
	5	3	3
	6	6 (REPLIC.)	4

PILOT EXPERIENCE PARAMETER (PE):

PILOT NO.	PILOT	IFR LOGGED FLIGHT HOURS/TOTAL TIME	PE = $\frac{\text{IFR TIME}}{600}$
1	B. NIXON	600/5000	1.00
2	D. PEOPLES	270/2500	0.45
3	NASA	-	

- O TRACK AND CONFIGURATION RANDOMIZATION
- O LEARNING CURVE EFFECT

SPIFR ON-BOARD DIGITAL DATA ACQUISITION SYSTEM



Subjective performance indicators are the Pilot Opinion Ratings (PORs). CHR is the Cooper-Harper Performance scale and the workload scale has been developed by the M.I.T. man-machine laboratory.

We are examining both flight test segments characteristic of the SPIFR regime and overall mission performance. This provides additional insight and augments the statistical basis.

EVALUATION SHEET

MISSION VARIANT #

CONFIGURATION #

PILOT

DATE

SPEED RETRIMMING

CHR

WORKLOAD

COMMENTS

HOLDING PATTERN

CHR

WORKLOAD

COMMENTS

GLIDE SLOPE TRACKING

CHR

WORKLOAD

COMMENTS

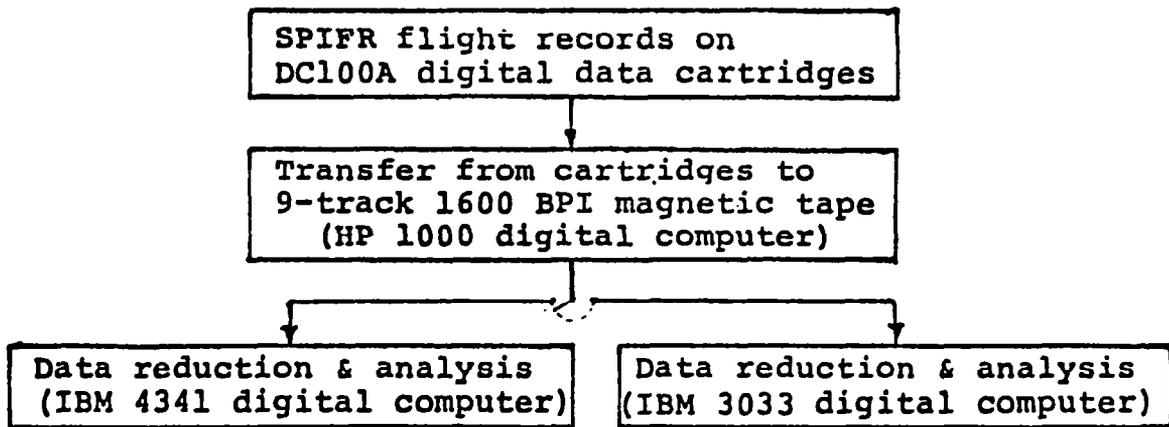
OVERALL MISSION

CHR

WORKLOAD

COMMENTS

OBJECTIVE DATA PREPROCESSING



- 0 CONVERSION OF 16-BIT BINARY DATA INTO DECIMAL INTEGERS
- 0 PHYSICAL TIME VECTOR FORMATTING
- 0 CONVERSION INTO VOLTAGE
- 0 CONVERSION INTO ENGINEERING UNITS

As the mathematical model is nonlinear, the extended Kalman filter is employed. The stabilized Kalman filter formulation is implemented to provide numerical robustness.

Bias-type states account for directional gyro bias and drift, for the DME range error and for the low frequency wind gusts. The geoid geometry and Earth rotation effects are incorporated in the model.

The system model has been divided into angular and translational submodels, which may be addressed sequentially, thus augmenting the numerical robustness. The filter tuning methodology takes advantage of the model division. It applies theoretical considerations and interacts with the SPIFR generic simulation.

OPTIMAL FLIGHT PATH RECONSTRUCTION

- 0 EXTENDED, STABILIZED KALMAN FILTER
- 0 RAUCH-TUNG-STRIEBEL OPTIMAL SMOOTHER
- 0 BIAS-TYPE STATES AND NAVIGATIONAL ASPECTS
(MATHEMATICAL MODEL EXTENSION)
- 0 ANALYTICAL DERIVATION OF STATE AND OBSERVATION JACOBIAN MATRICES
- 0 DIVISION INTO LOWER-ORDER SUBMODELS
- 0 SEQUENTIAL COMPLEMENTARY FILTER TUNING

The optimal smoother algorithm improves both the state estimates and the associated covariances. Bias-type states may cause significant estimation errors if their wide-range variations are not accounted for.

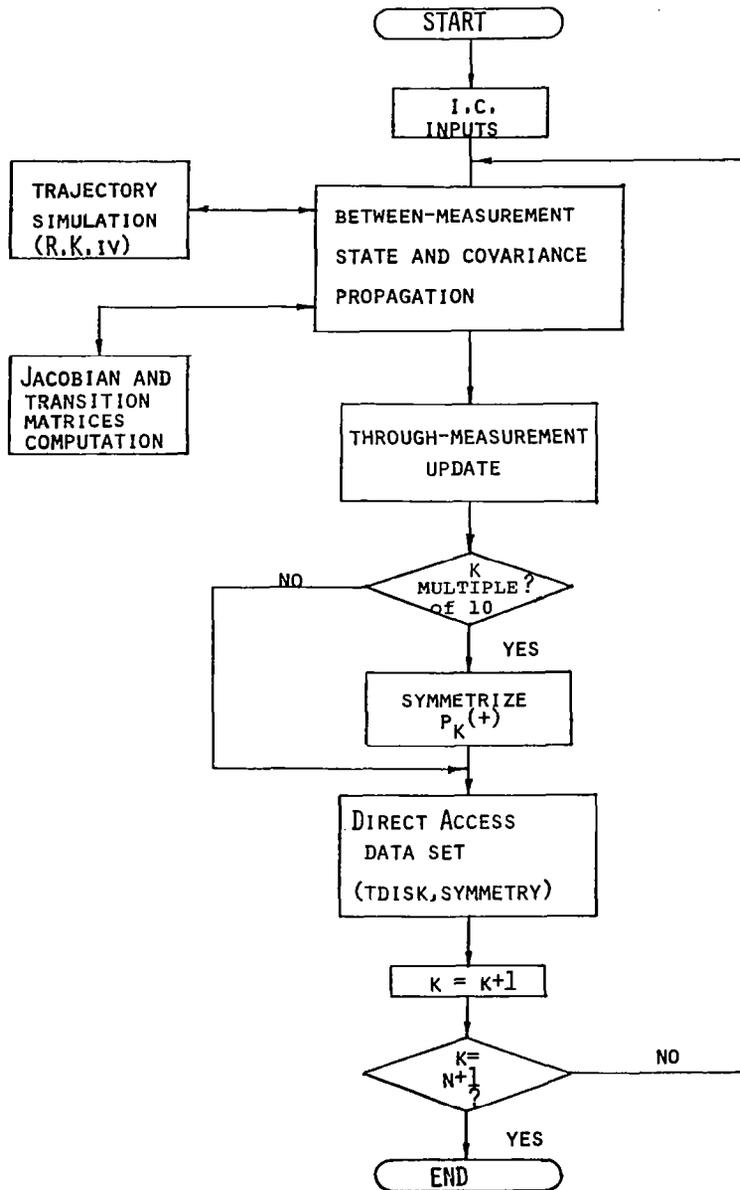
DESIGN AND ANALYSIS OF THE OPTIMAL SMOOTHER

- 0 FILTER SENSITIVITY ANALYSIS

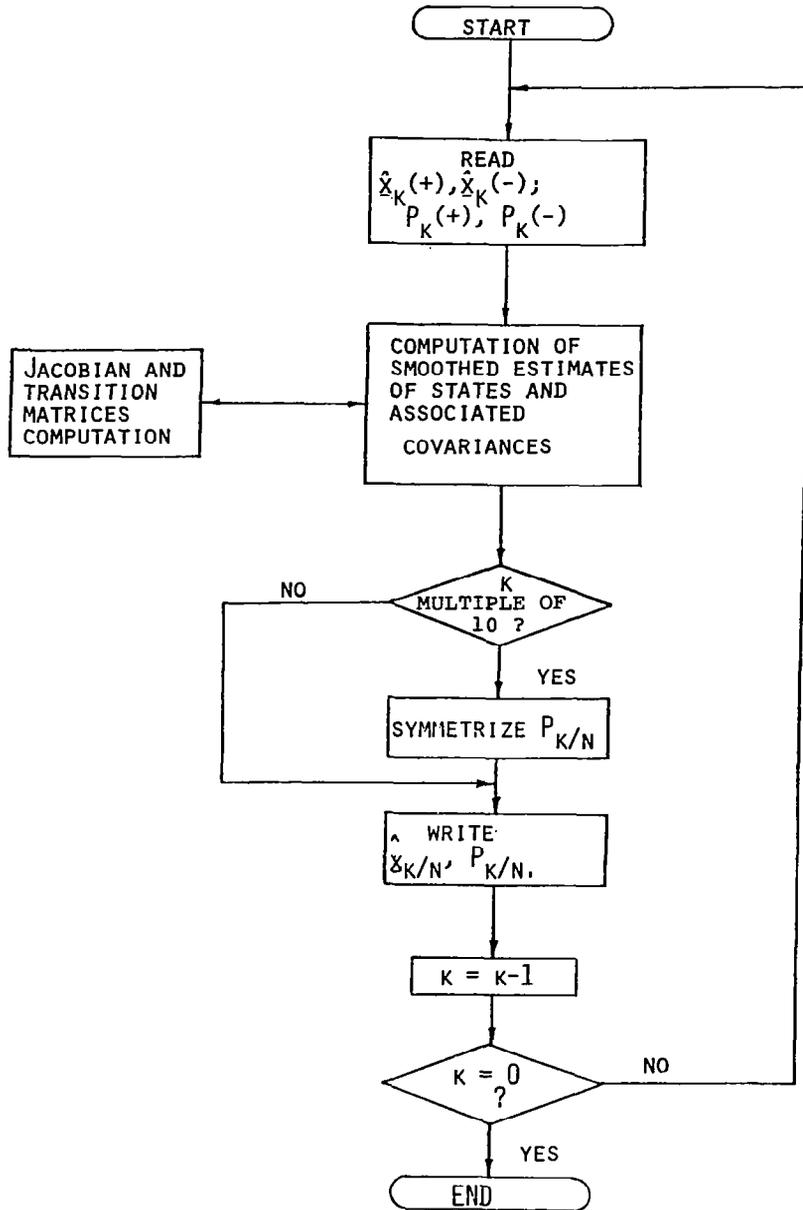
- 0 IMPLEMENTATION ISSUES (DATA COMPRESSION, NONSIMULTANEOUS DME LOCK-ON, OUTLIERS)

- 0 INTERACTION WITH PREFLIGHT AND FLIGHT-TESTING PROCEDURE (BIASES EXTRACTION, MISSION STARTING POINT)

FORWARD FILTERING PROGRAM



BACKWARD SMOOTHING PROGRAM



With regard to the pitch angle and yaw rate time histories, "derivative" states are noisier than "integral" states, as may have been expected.

OPTIMAL FLIGHT PATH RECONSTRUCTION - INPUTS

- DATA RECORD LENGTH
- TIME VECTORS OF CODES IDENTIFYING THE GROUND STATIONS

STATION CODE	STATION	$N 40^{\circ} X'$	$W 074^{\circ} Y'$	Z_I (FT)
1	RBV	12.1	29.7	-250.
2	COL	18.7	09.6	-120.
3	GXU	00.6	35.8	-120.
4	SBJ	35.0	44.5	-190.

0	FORR.	20.8	36.6	-109.

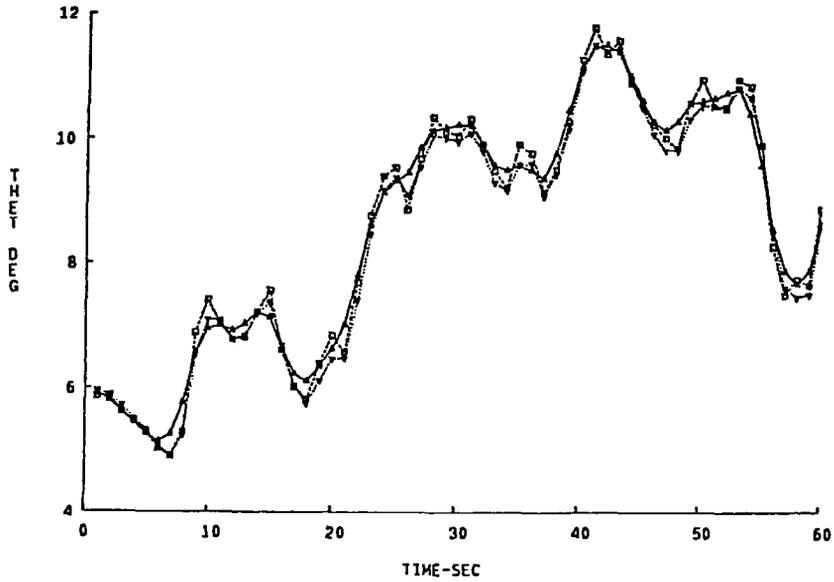
CHANNEL DEDICATED TO STATION SWITCHING TIMING

NAV2 \ NAV1	RBV	COL	GXU	SBJ
RBV	EE	ED	EB	E7
COL	DE	DD	DB	D7
GXU	BE	BD	BB	B7
SBJ	7E	7D	7B	77

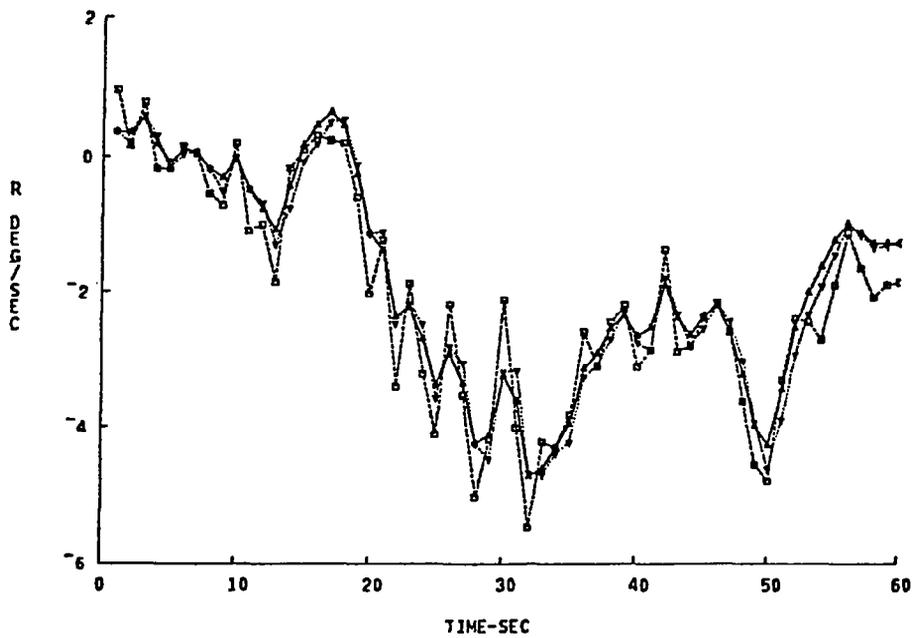
- APPROXIMATE INITIAL CONDITIONS

APPLICATION OF OPTIMAL FLIGHT PATH RECONSTRUCTION
ALGORITHM TO ACTUAL FLIGHT-TEST DATA

PITCH ANGLE SMOOTHING (SEPT.17, 1981)

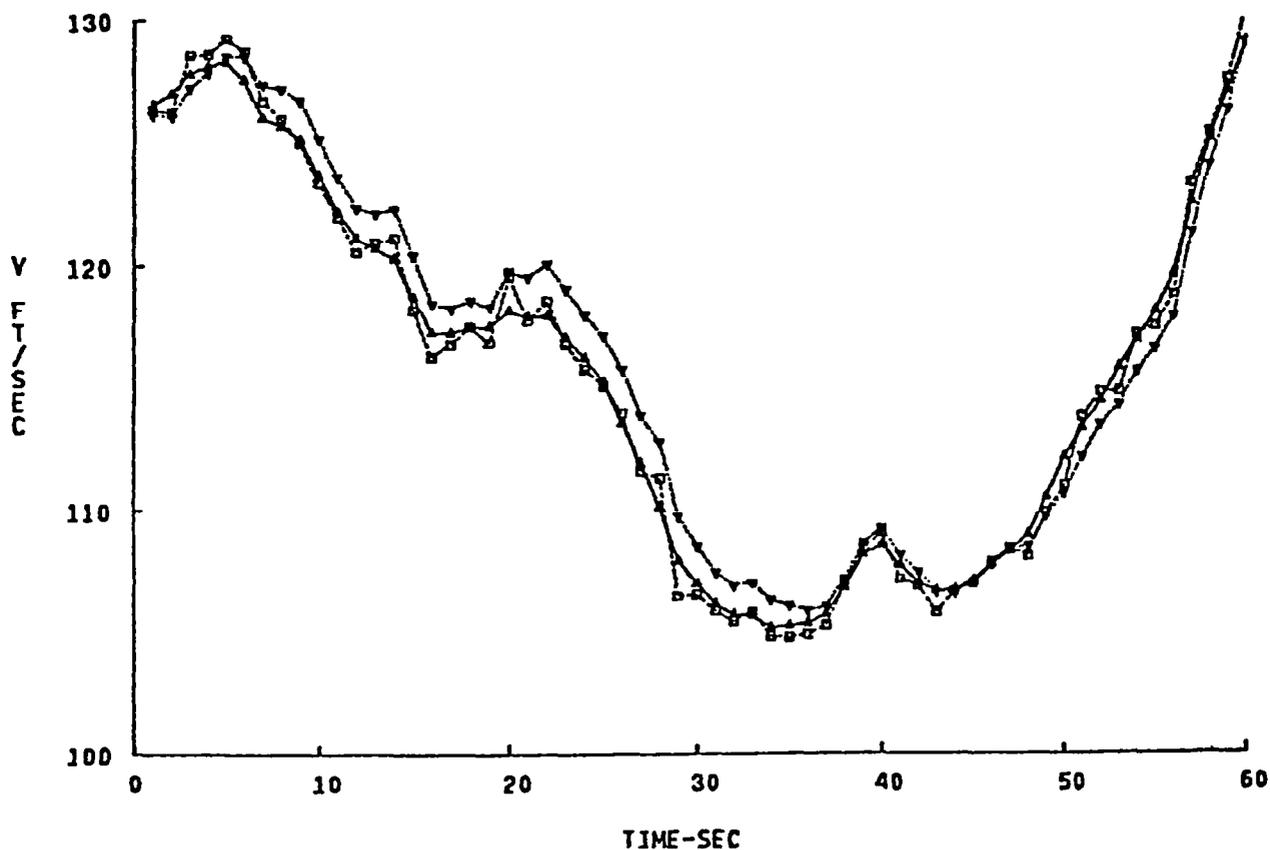


YAW RATE SMOOTHING (SEPT. 17, 1981)



With regard to the true airspeed time history, note demonstration of characteristic filter lag, which is corrected by the smoother. This is a reconstructed measurement from the $[u,v,w]^T$ states.

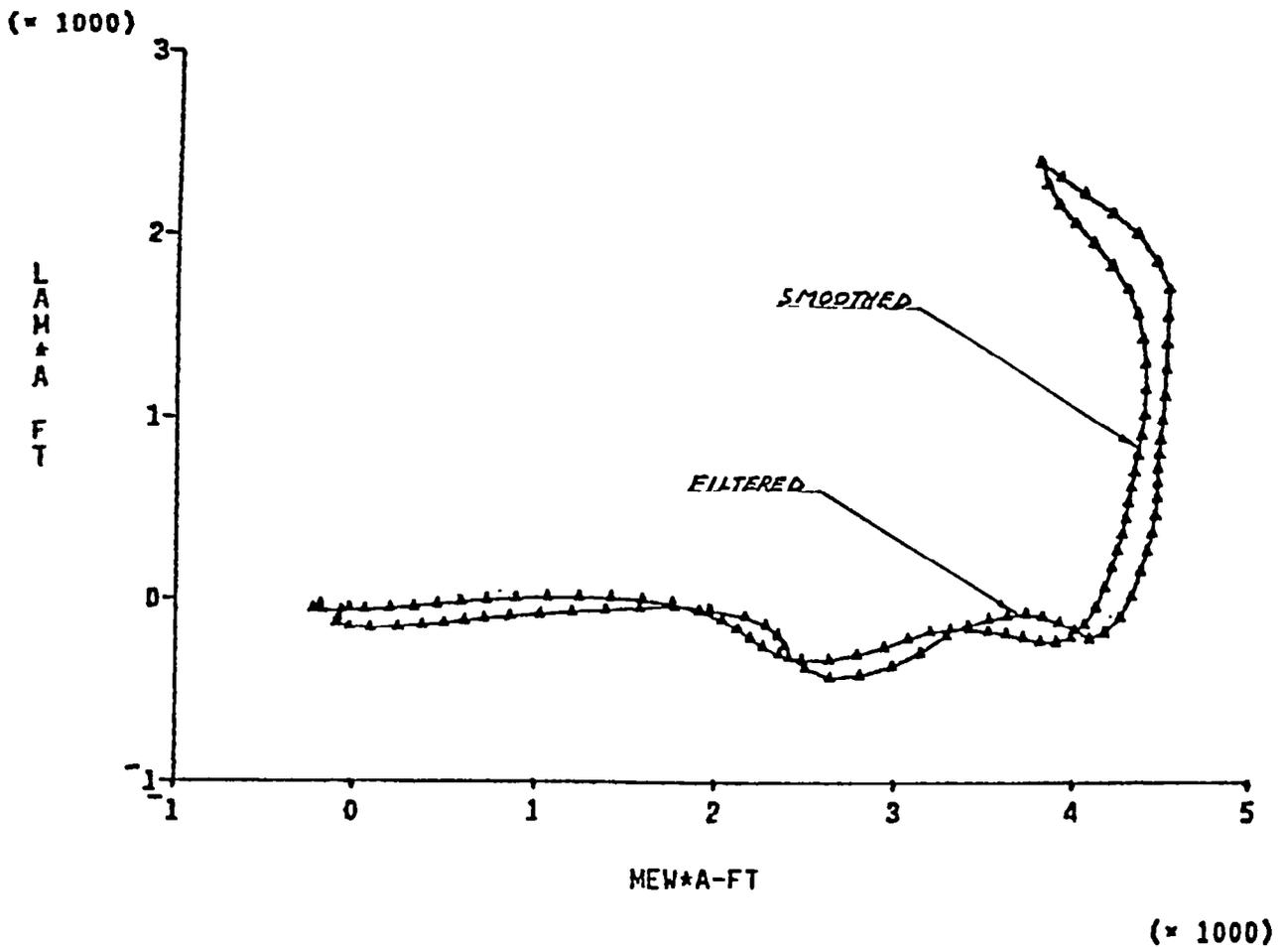
TRUE AIRSPEED RECONSTRUCTION (SEPT. 17, 1981)



With regard to the trajectory reconstruction, note that optimal smoothing improves the state estimates and at the same time also shrinks the statistical uncertainty ellipsoid.

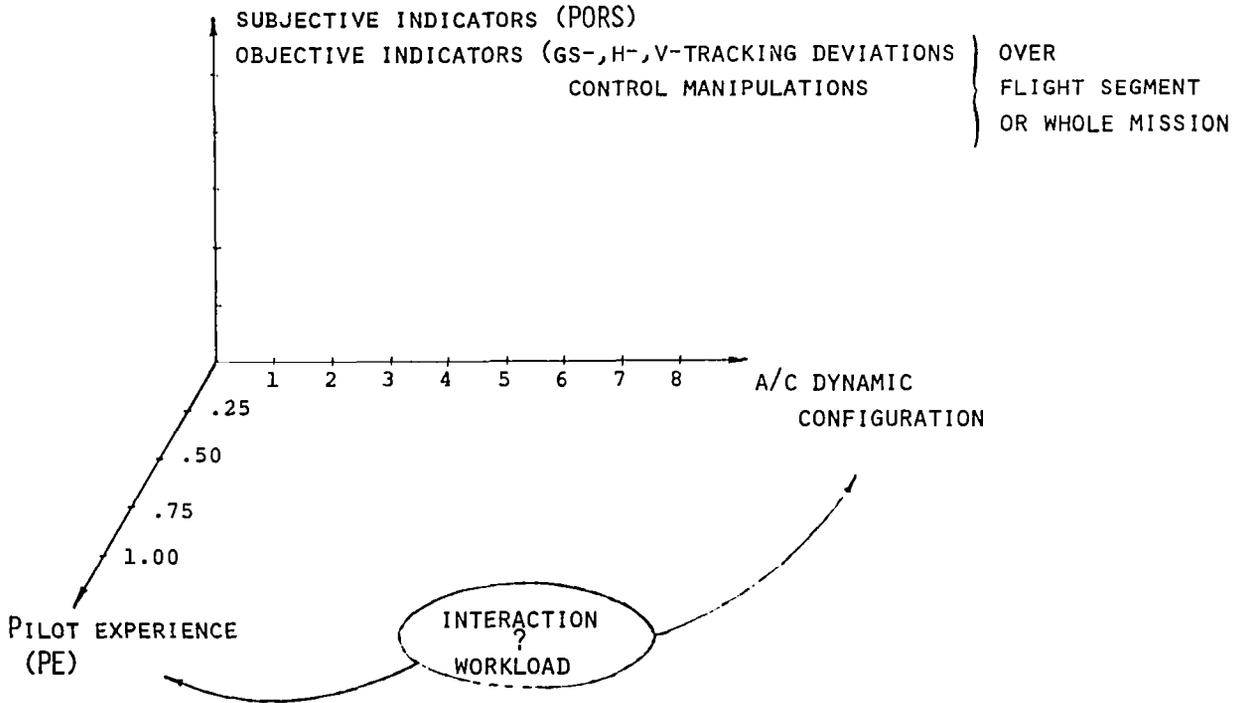
Note: Line segments are used to link results but not to suggest a functional relationship.

TRAJECTORY RECONSTRUCTION (SEPT. 17, 1981)



This post-flight flight path reconstruction approach may be useful in evaluating navigational system performance (on board the TCV, e.g.) or to investigate statistically causes of flight path deviations if recording altitude, airspeed, and DME data in the "black box".

SPIFR MULTIPLE REGRESSION ANALYSIS (PHASE I)



WORK ACCOMPLISHED TO DATE

- 0 INTEGRATED FLIGHT TESTING AND FLIGHT PATH RECONSTRUCTION
METHODOLOGY DEVELOPED

- 0 HIGH ACCURACY IN TRAJECTORY ESTIMATION ACHIEVED WITH AN
INEXPENSIVE EXPERIMENTAL SETUP

- 0 PART OF FLIGHT TEST SERIES FLOWN

AIR DATA MEASUREMENT USING
DISTRIBUTED PROCESSING AND
FIBER OPTICS DATA TRANSMISSION

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PRINCETON UNIVERSITY

A DUAL REDUNDANT AIR DATA MEASUREMENT SYSTEM INCORPORATING DISTRIBUTED
PROCESSING AND FIBER OPTIC DATA BUSES

OVERALL RESEARCH GOAL:

GAIN EXPERIENCE WITH --DISTRIBUTED PROCESSING
--FIBER OPTIC TECHNOLOGY AND
--REDUNDANCY MANAGEMENT
IN THE AIRCRAFT ENVIRONMENT.

THIS PROJECT:

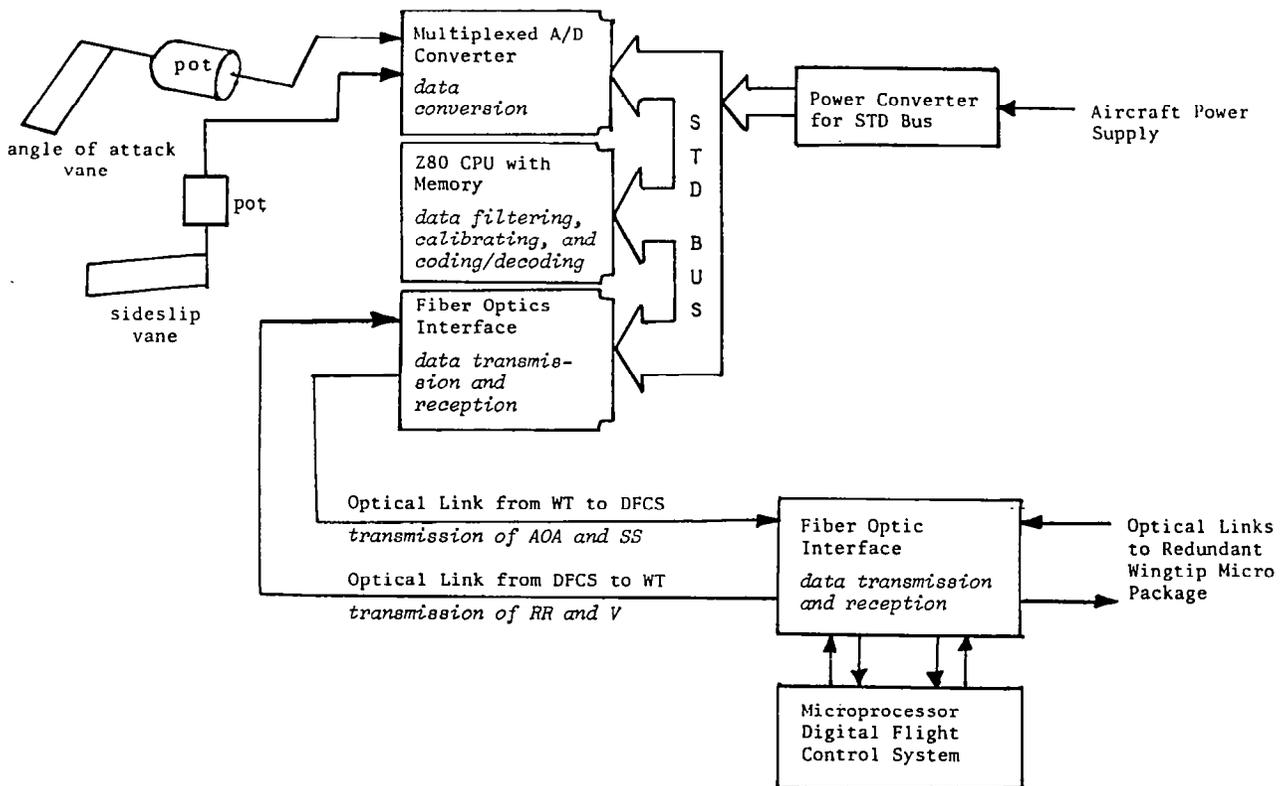
DEVELOPMENT OF AN ANGLE OF ATTACK AND SIDESLIP DATA COLLECTION SYSTEM WHICH
FEATURES:

- TWO INDEPENDENT MICROPROCESSOR-CONTROLLED DATA
COLLECTION AND CALIBRATION UNITS
- TRANSMISSION OF DATA TO THE CONTROL SYSTEM ON A
FIBER OPTIC DATA BUS
- SOFTWARE-IMPLEMENTED ERROR DETECTION AND RECOVERY

AIR DATA MEASUREMENT SYSTEM

This figure shows a functional breakdown of the entire system.

Two air data sensor vanes -- measuring angle of attack and sideslip angle -- are mounted at each wingtip of the aircraft. Their analog output signal is converted to digital format by a multiplexed A/D converter. Next, any signal noise and other unwanted contributions such as upwash and roll are eliminated from the raw data by software-implemented filtering and calibration, so that each wingtip sensor unit's data is independent of the other's, thus giving the system dual redundancy. Finally, the data are transferred via a fiber optic data link to the aircraft's digital flight control system, which uses the system's dual redundancy to determine the data's validity before using it as inputs to the flight control system.



EQUIPMENT INSTALLED IN AIRCRAFT

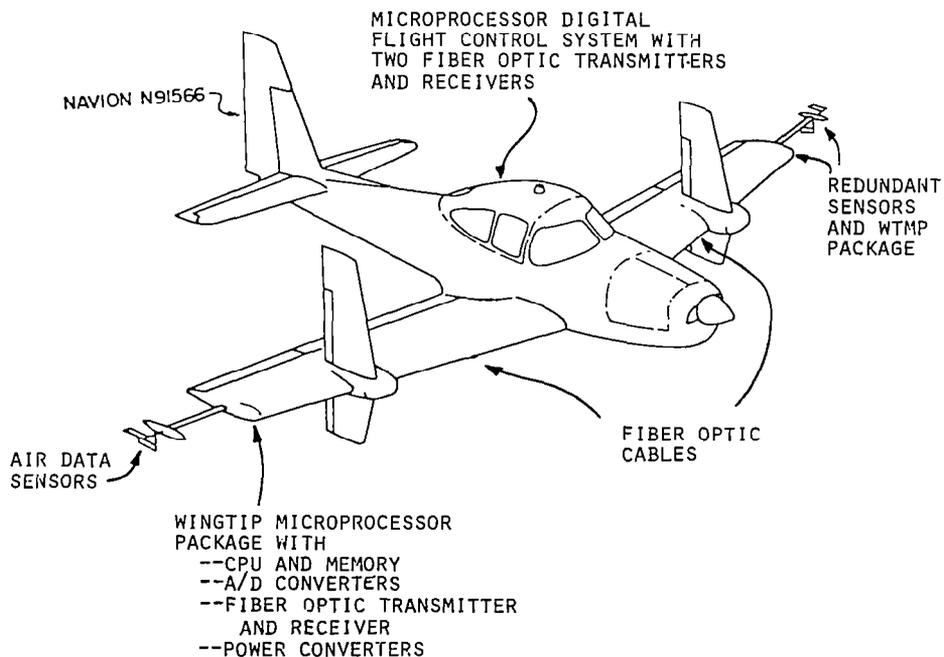
This figure shows the location of the equipment in the aircraft.

WINGTIP MICROPROCESSOR PACKAGE:

Card cage and microprocessor bus --
Prolog STD (56-pin, tightly structured bus).
CPU and memory --
Mostek MDX-CPU2 (4 MHz Z80 CPU with byte-wide interchangeable RAM, PROM, and ROM).
A/D converters --
Data Translation DT2742 (12-bit converter with 8 differential input channel multiplexing capability).
Fiber optic interface --
Optelecom 2100 series fiber optic transmitter and receiver mounted on a Prolog Utility I/O card.
Power supply --
Power Products DC-DC converters (28 vdc to 5 vdc and \pm 12 vdc).

FIBER OPTIC LINKS:

Cables --
Siecor 155 (200 micron core all-glass fiber in rugged sheathing).
Connectors --
Epoxy Technology SMA (all-metal epoxy-bonded connectors).



DATA COMMUNICATIONS STRUCTURE

This air data measurement system uses two microprocessors loosely coupled to a third, the micro-DFCS, which is the executive processor of the system.

The traffic management scheme chosen for data exchanges between the microprocessors is a modified polling system. The micro-DFCS interrupts the wingtip microprocessors whenever angle-of-attack or sideslip data is needed and whenever roll rate and velocity data is available. The wingtip microprocessors cannot interrupt the micro-DFCS, however, since uncontrolled delays in some flight control routines might be undesirable. This bus protocol minimizes the data communications overhead for all processors, the timing sensitivity, and the propagation of wingtip microprocessor problems to the micro-DFCS.

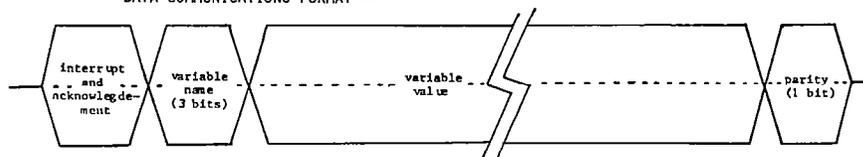
To further simplify timing, each data point transmitted is accompanied by a name. Transmission of a parity bit enables the receiving processor to identify most transmission errors.

The code used in transmitting data is Manchester Bi-Phase, also known as self-clocking return-to-zero (RZ) code. The beginning of each bit interval is marked by a transition. If the bit is a one, a second transition will occur in the middle of the interval; for a zero bit, the signal will remain at the same level throughout the interval. This code requires twice the bandwidth of more commonly used non-return-to-zero code schemes, but eliminates many of their timing problems and lengthens transmitter life.

TRAFFIC MANAGEMENT -- POLLING

μDFCS INTERRUPTS THE WINGTIP MICROPROCESSORS WHENEVER DATA IS NEEDED OR AVAILABLE.

DATA COMMUNICATIONS FORMAT --



CODE TYPE --

BI-PHASE SELF-CLOCKING



FLIGHT TESTING

Flight testing of this system will be divided into two phases: hardware evaluation and total system evaluation.

The primary goal of the first phase is verifying that all the system hardware performs satisfactorily in flight. These tests will be done with a minimum of software so that hardware faults can be easily separated from software bugs. Of course, the communications hardware cannot be adequately tested without the data communications software, so the data communications techniques just described will be tested simultaneously. A secondary task scheduled in this part of the testing is collecting some data to check the analytically estimated calibration coefficients to be used in the system later.

The second phase of the tests, total system evaluation, will focus on verifying the data filtering and calibration software as well as the system's fault tolerance. Performance criteria for this phase include the accuracy of the calibration and the degree of isolation of each sensor unit.

OBJECTIVES

1) HARDWARE TECHNOLOGY EVALUATION

--TEST OF HARDWARE AND DATA TRANSMISSION TECHNIQUE

--COLLECTION OF DATA TO CHECK CALIBRATION COEFFICIENT ESTIMATES

2) TOTAL SYSTEM EVALUATION

--TEST OF DATA FILTERING AND CALIBRATION SOFTWARE

--TEST OF SOFTWARE-IMPLEMENTED FAULT TOLERANCE

PROGRESS SUMMARY

PREVIOUS--

- FIBER OPTIC LINKS DESIGNED, ASSEMBLED, AND GROUND TESTED
- MICROPROCESSOR, A/D, AND POWER HARDWARE ACQUIRED
- SOFTWARE PARTIALLY COMPLETE

THIS PERIOD--

- FIBER OPTIC/ MICROPROCESSOR INTERFACES DESIGNED, ASSEMBLED, AND GROUND TESTED
- MICROPROCESSOR, A/D, AND POWER HARDWARE GROUND-TESTED OUTSIDE THE AIRCRAFT
- ALL HARDWARE INSTALLED IN THE AIRCRAFT AND GROUND-TESTED IN POSITION
- TRANSMISSION SOFTWARE GROUND TESTING IN PROGRESS
- CALIBRATION AND FILTERING SOFTWARE STILL IN DEVELOPMENT

FUTURE WORK--

- EVALUATE ALL HARDWARE AND DATA TRANSMISSION IN FLIGHT
- FINISH DATA FILTERING AND CALIBRATION SOFTWARE
- GROUND TEST SYSTEM WITH FILTERING AND CALIBRATION SOFTWARE ADDED
- FLIGHT TEST COMPLETE SYSTEM



INPUT/OUTPUT MODELS FOR GENERAL
AVIATION PISTON-PROP AIRCRAFT FUEL ECONOMY

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A FUEL-EFFICIENT CRUISE PERFORMANCE MODEL
FOR GENERAL AVIATION PISTON ENGINE AIRPLANES

SPECIFIC RANGE = R^*
 = GROUND MILES/LB FUEL
 = INSTANTANEOUS FUEL ECONOMY

FIXED WING GA AIRPLANES

- FIXED DESIGN
- NATURALLY ASPIRATED SI PISTON ENGINES
- CONSTANT SPEED PROPELLERS
- MAXIMIZE R^* USING AVIONICS AND CONTROLS

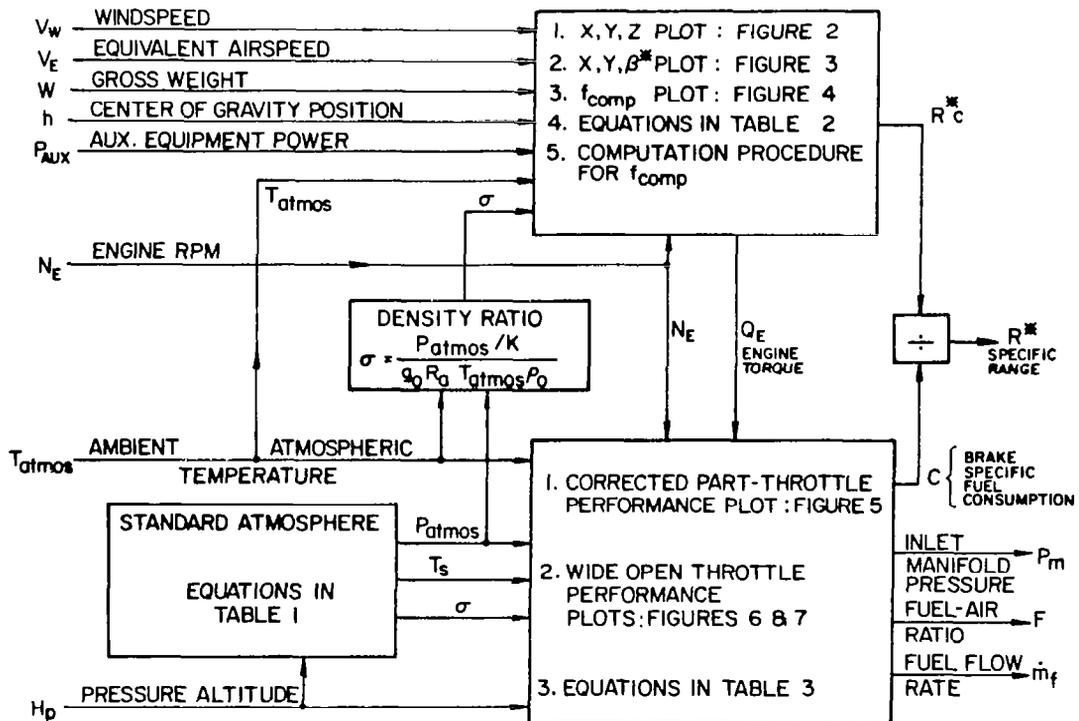


Figure 1. Block diagram: Cruise performance model (standard and nonstandard atmospheres).

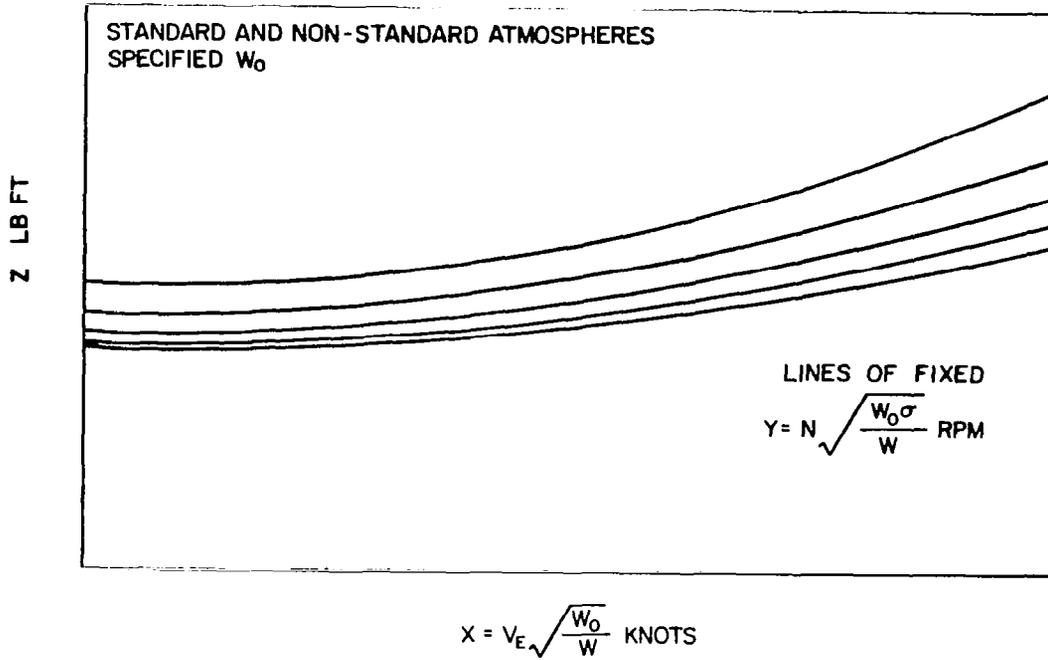


Figure 2. X,Y,Z plot: Airframe-propeller performance.

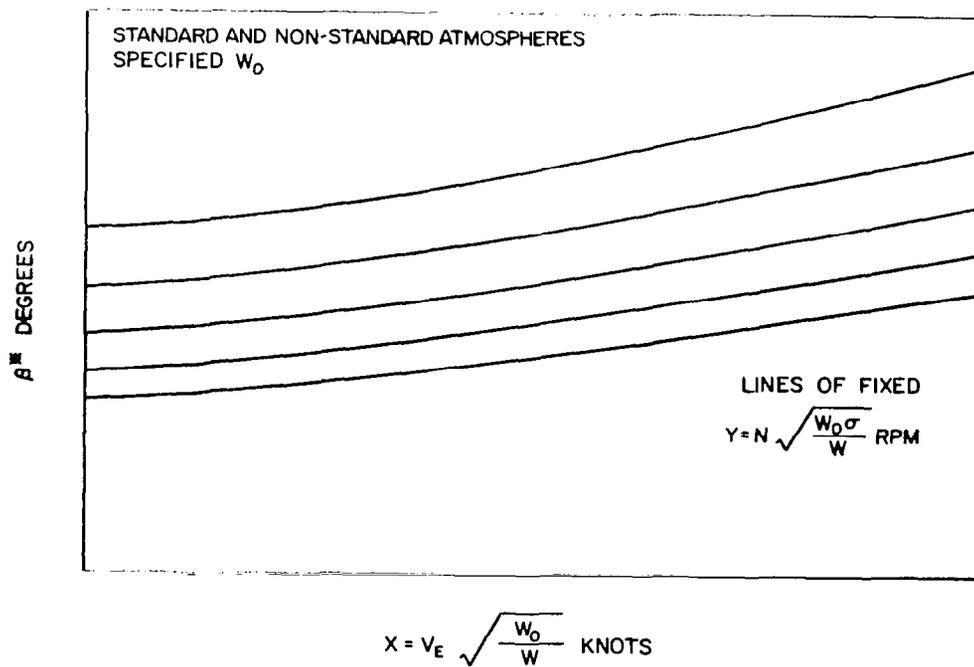


Figure 3. X,Y, β^* plot: Airframe-propeller performance.

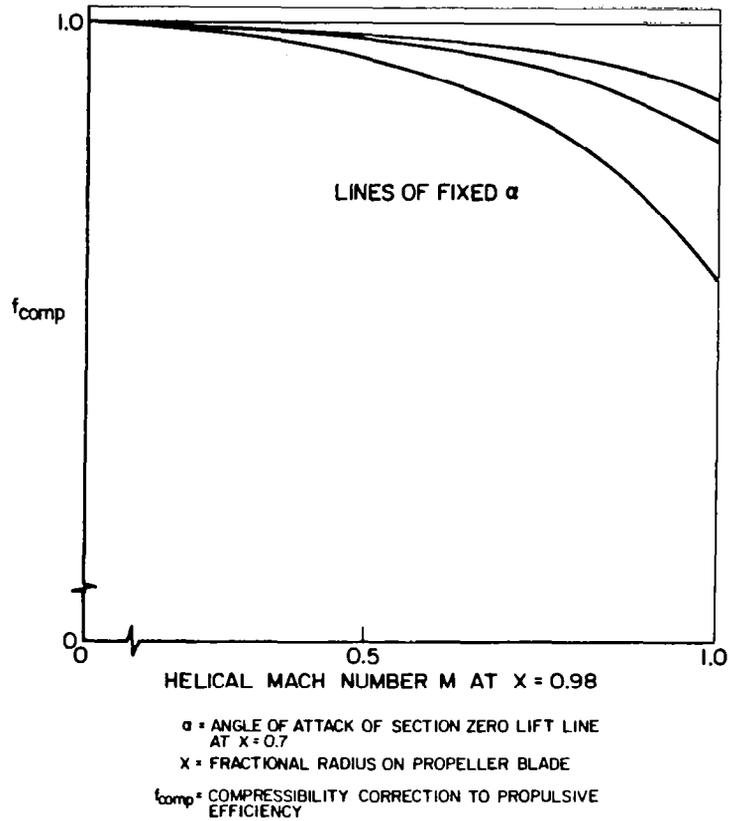


Figure 4. Propeller performance: Compressibility correction f_{comp} plot.

TABLE 1.
EQUATIONS FOR THE STANDARD ATMOSPHERE

These equations approximate the characteristics of the U.S. Standard Atmosphere 1962 in the troposphere.

$$H = H_p \quad (1.1)$$

$$\theta = 1 - 6.87239 \times 10^{-6} H \quad (1.2)$$

$$\delta = \theta^{5.25581} \quad (1.3)$$

$$\sigma = \frac{\rho}{\rho_0} = \frac{\delta}{\theta} \quad (1.4)$$

$$T_s = 288.15 \theta \quad (1.5)$$

$$P_{atmos} = 29.92 \delta \quad (1.6)$$

TABLE 2

EQUATIONS FOR AIRFRAME-PROPELLER-ATMOSPHERE CRUISE PERFORMANCE

$$V_e = 1.6889 V_E \quad (2.1)$$

$$C_L = 2W/\rho_o V_e^2 S \quad (2.2)$$

$$P_{AUX_c} = P_{AUX} \sqrt{W_o^3 \sigma / W^3} \quad (2.3)$$

$$V_{w_c} = V_w \sqrt{W_o \sigma / W} \quad (2.4)$$

$$X = V_E \sqrt{W_o / W} \quad (2.5)$$

$$Y = N \sqrt{W_o \sigma / W} \quad (2.6)$$

$$S^* = \frac{5252.1}{E} \frac{X}{YZ} \frac{W_o}{W} \quad (2.7)$$

$$\psi = AB^* - B \quad (2.8)$$

$$\Delta B = C \cos \psi \sin \left(\psi - \frac{D}{|dh|} \right) [(1 + \xi C_L dh)^k - 1] \quad (2.9)$$

$$B = B^* + \Delta B \quad (2.10)$$

$$Q_a = \frac{WZ}{W_o (1 + \xi C_L dh) f_{comp}} \quad (2.11)$$

$$\Lambda = 1 + 5252.1 (1 + \xi C_L dh) f_{comp} \left[\frac{P_{AUX_c}}{YZ} \right] \quad (2.12)$$

$$N_E = G N \quad (2.13)$$

$$[Q_E]_{APA} = Q_a \Lambda / G \quad (2.14)$$

$$R^* c = \left[1 + \frac{V_{w_c}}{X} \right] \frac{(1 + \xi C_L dh) f_{comp} S^*}{\Lambda} \quad (2.15)$$

Note: B is required for computing f_{comp} .

NATURALLY ASPIRATED SI ENGINE
MBT IGNITION TIMING

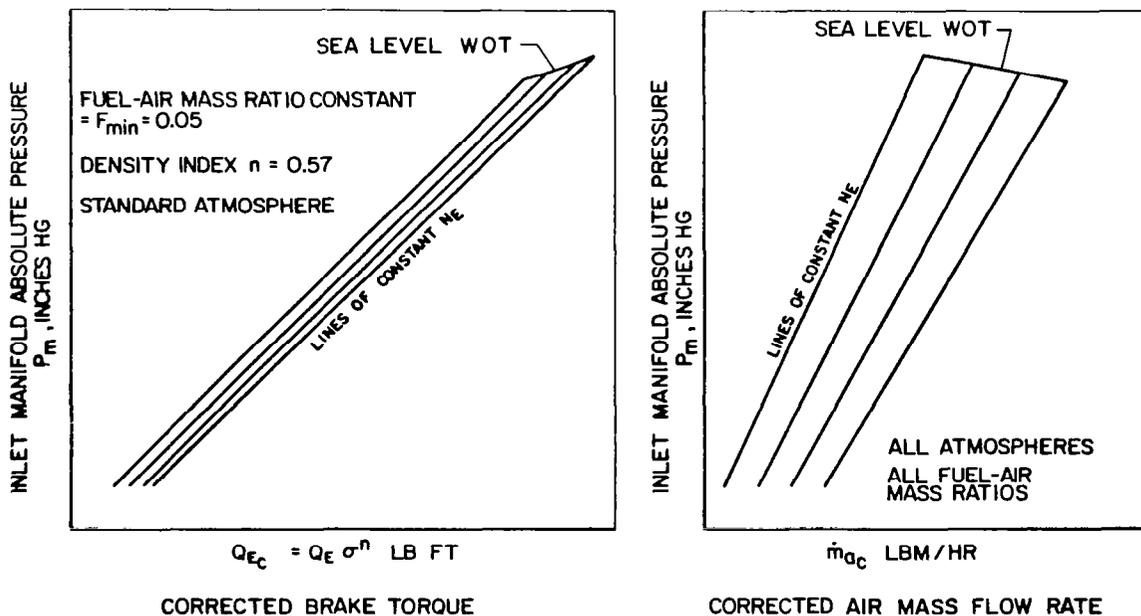


Figure 5. Corrected part-throttle engine performance.

NATURALLY ASPIRATED SI ENGINE WITH MBT IGNITION TIMING

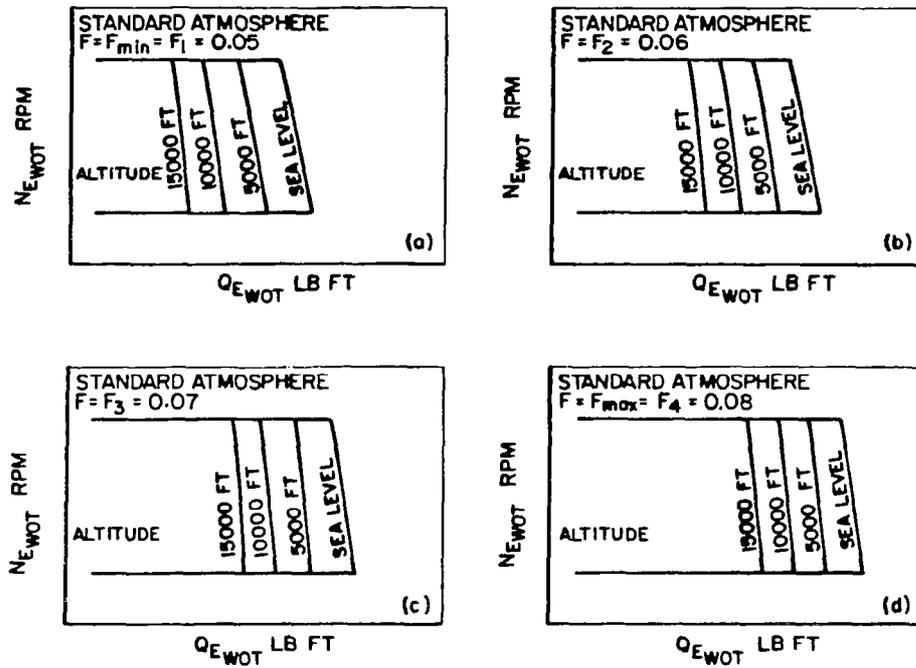


Figure 6. Wide open throttle performance: Engine shaft speed N_{EWOT} versus engine brake torque Q_{EWOT} .

NATURALLY ASPIRATED SI ENGINE WITH MBT IGNITION TIMING

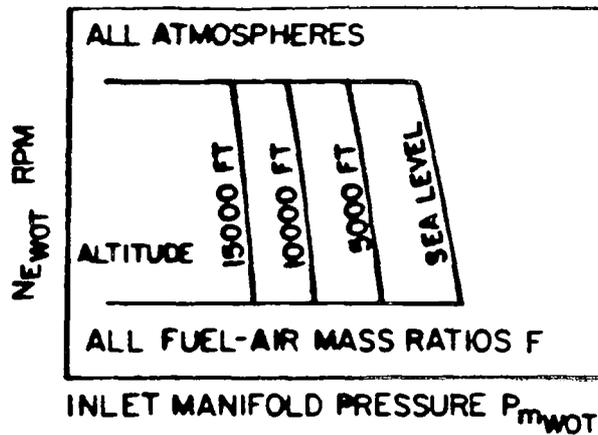


Figure 7. Wide open throttle performance: Engine shaft speed N_{EWOT} versus inlet manifold absolute pressure.

TABLE 3.

EQUATIONS FOR NATURALLY ASPIRATED ENGINE CRUISE PERFORMANCE

$$\Delta T_{atmos} = T_{atmos} - T_s \quad (3.1)$$

$$Q_E = [Q_E]_{APA} - \left[\frac{\partial Q_E}{\partial T_{atmos}} \right] \Delta T_{atmos} \quad (3.2)$$

$$Q_{Ec} = Q_E \sigma^n \quad (3.3)$$

$$\dot{m}_a c = \dot{m}_a \left[\frac{T_{atmos}}{288.15} \right]^{(1-\epsilon_t)} \left[\frac{P_{atmos}}{29.92} \right]^{\epsilon_p} \quad (3.4)$$

$$\dot{m}_f = F \dot{m}_a \quad (3.5)$$

$$P_E = 2\pi [Q_E]_{APA} N_E / 33,000 \quad (3.6)$$

$$c = \dot{m}_f / P_E \quad (3.7)$$

SUMMARY

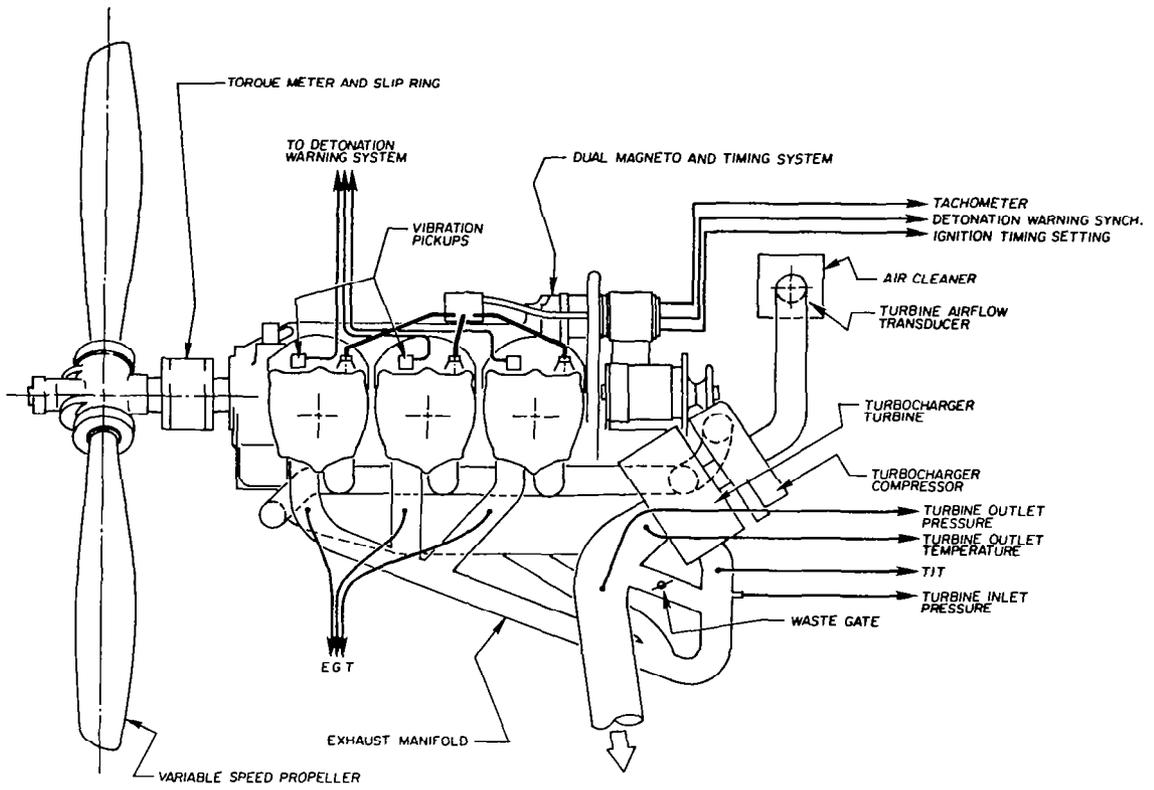
1. COMPACT CRUISE PERFORMANCE MODEL

- CORRECTED QUANTITIES
- CORRECTED PERFORMANCE PLOTS
- ALGEBRAIC EQUATIONS
- MAXIMIZE R* WITH OR WITHOUT CONSTRAINTS
- APPEARS SUITABLE FOR AIRBORNE MICROPROCESSOR IMPLEMENTATION

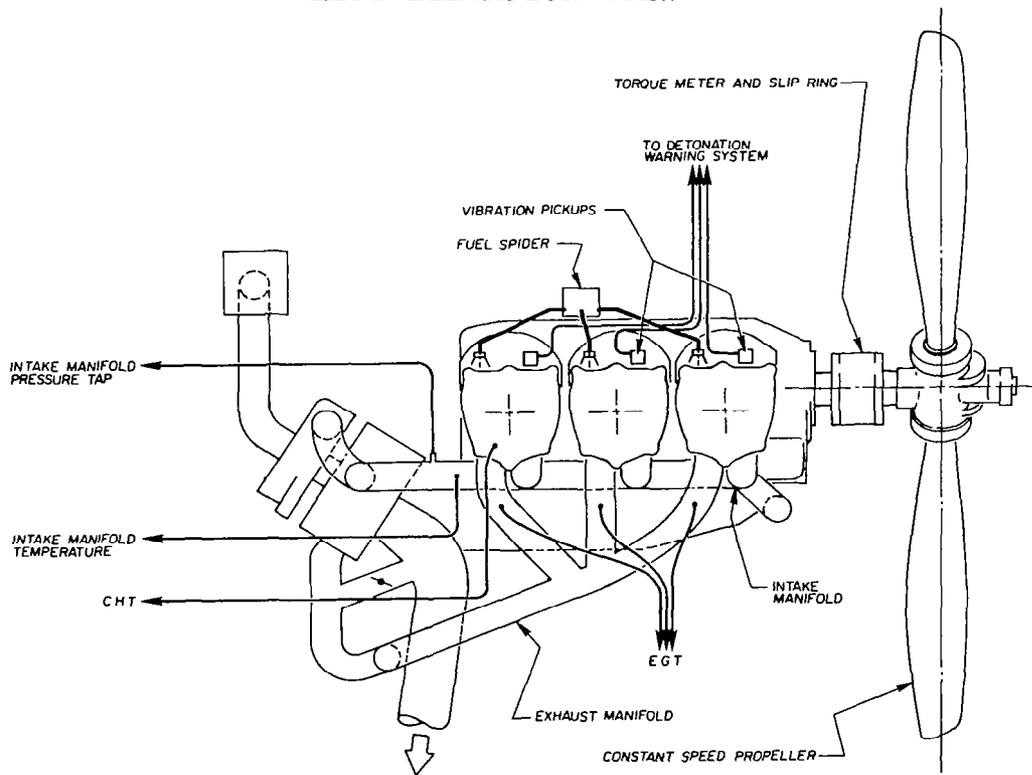
2. HARDWARE REQUIREMENTS

- IGNITION TIMING REGULATOR
- FUEL-AIR MASS RATIO CONTROLLER
- MICROPROCESSOR
- SENSORS AND DISPLAYS

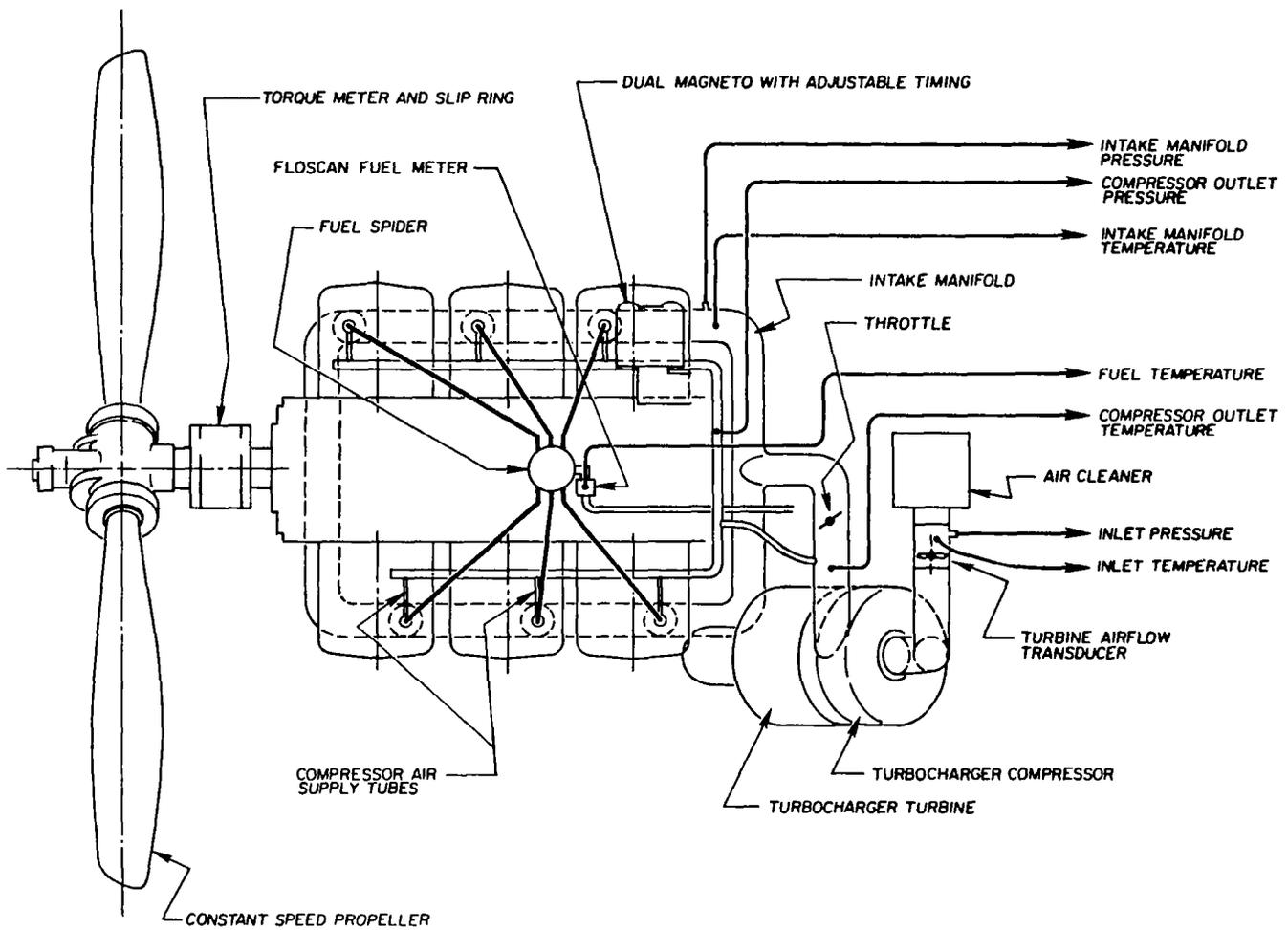
3. TYPICAL R* INCREASE = 20% TO 26% ABOVE CURRENTLY ACHIEVED R* VALUES.



LEFT ELEVATION VIEW



RIGHT ELEVATION VIEW



PLAN VIEW



WIDE FIELD OF VIEW LASER BEACON SYSTEM
FOR THREE DIMENSIONAL AIRCRAFT RANGE MEASUREMENTS

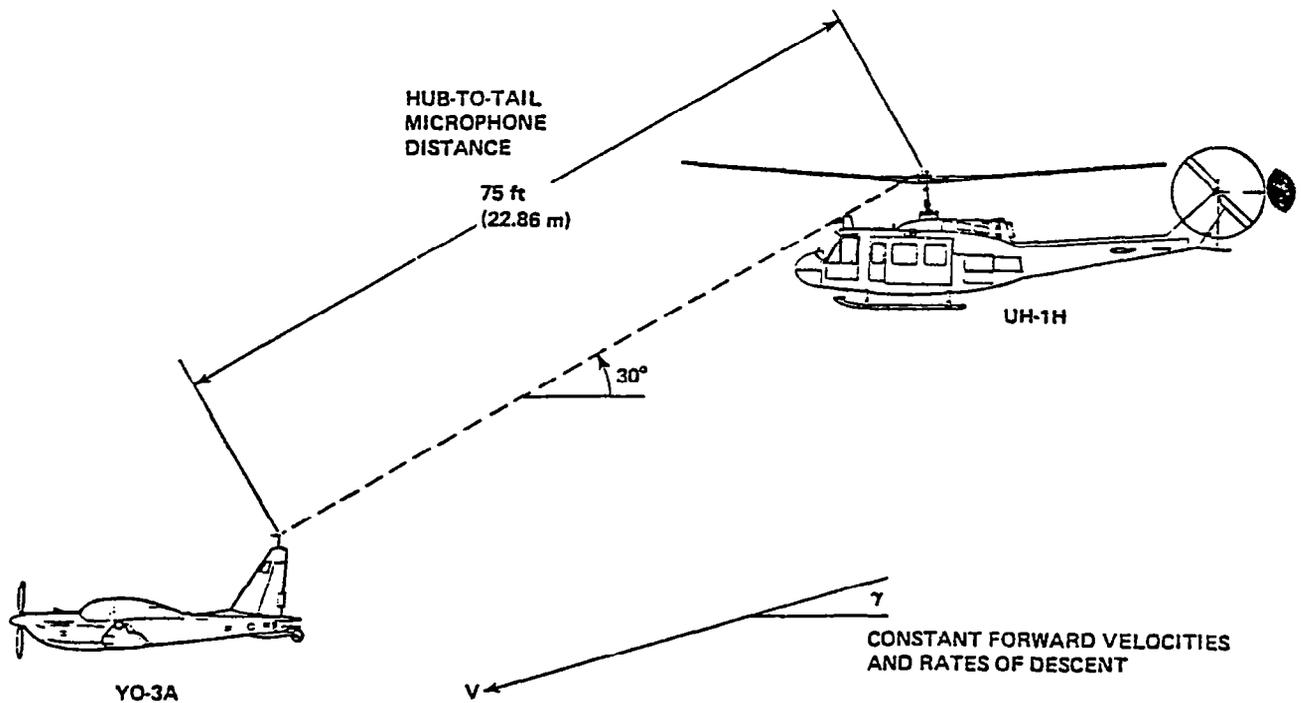
E. Y. WONG
PRINCETON UNIVERSITY

OBJECTIVE

This is a project for NASA Ames Research Center to develop a system that can measure accurately the distance from an aircraft to a helicopter for rotor noise flight testing. This system will be able to measure the range and angles between these two aircraft using laser optics. This system could be applied in areas such as collision avoidance, robotics, and other measurement-critical tasks.

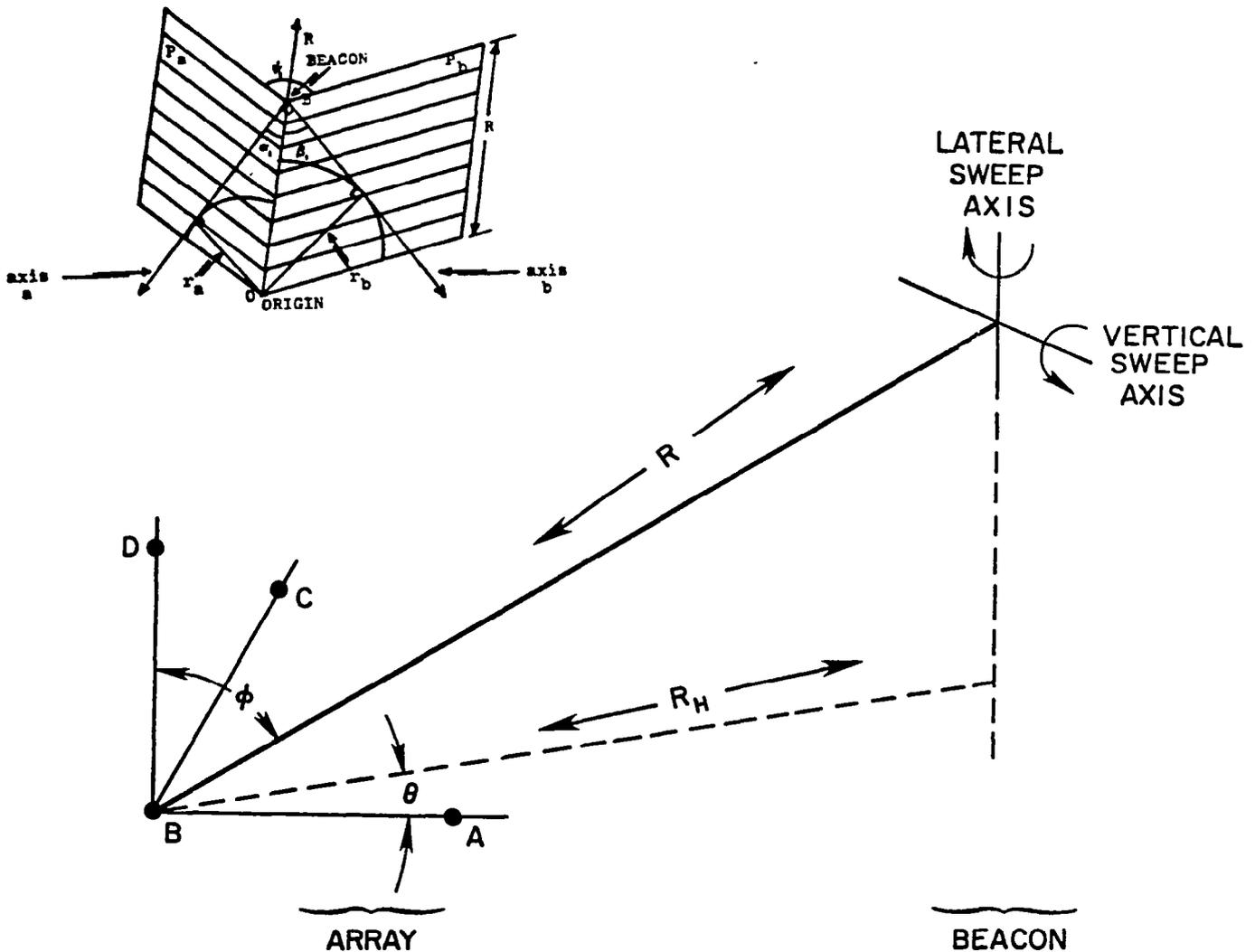
PRINCIPLES OF OPERATION

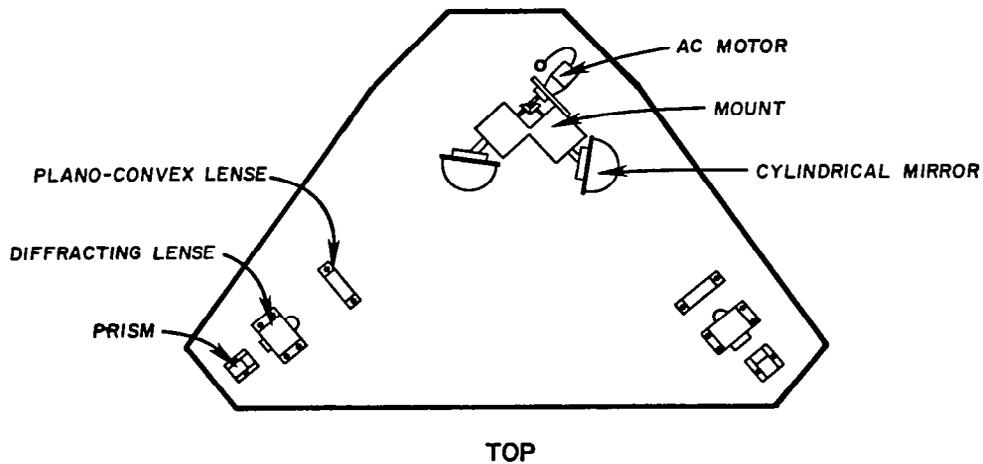
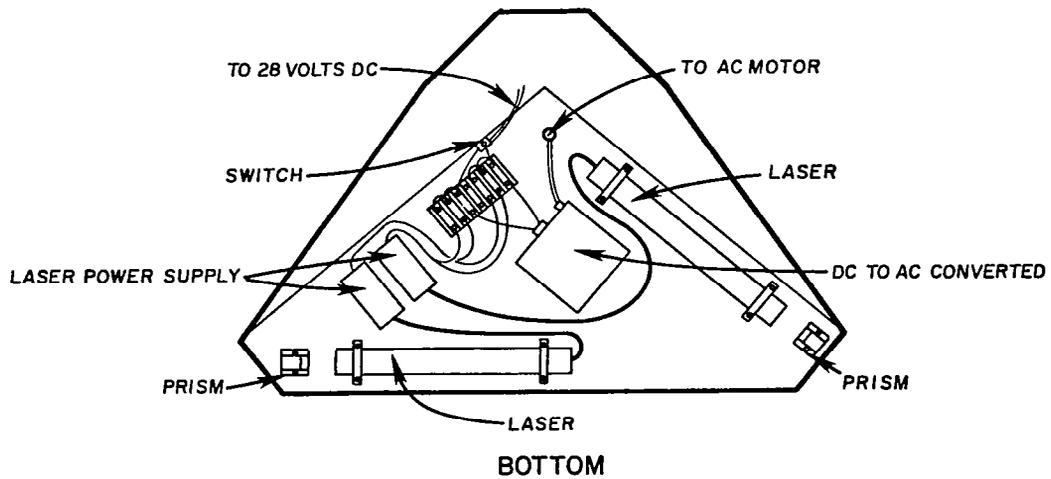
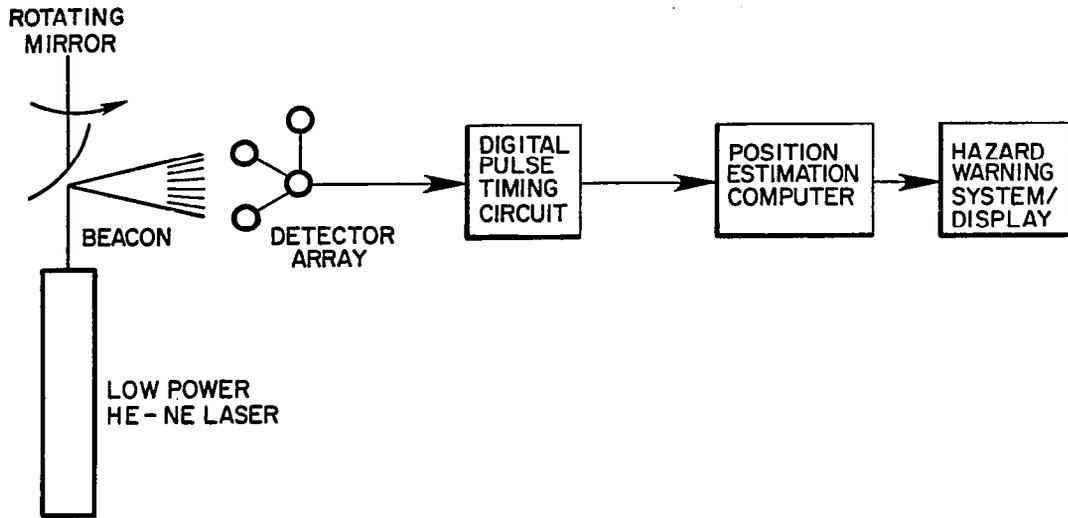
A laser beacon is mounted on the front of a helicopter which has a pair of sweeping orthogonal fan-shaped beams of laser light. This light passes a set of detectors that are mounted on the back of another aircraft, which receives a set of pulses on each sweep. These pulses determine the vector orientation of each rotating beam; using this pair of vectors the vector pointing from the array to the beacon can be found. True range measurements can be calculated once the sweep rate and array geometry are known. This position data is then displayed to the test engineer in the aircraft, and error signals are sent to the helicopter pilot.



LASER BEACON SUBSYSTEM

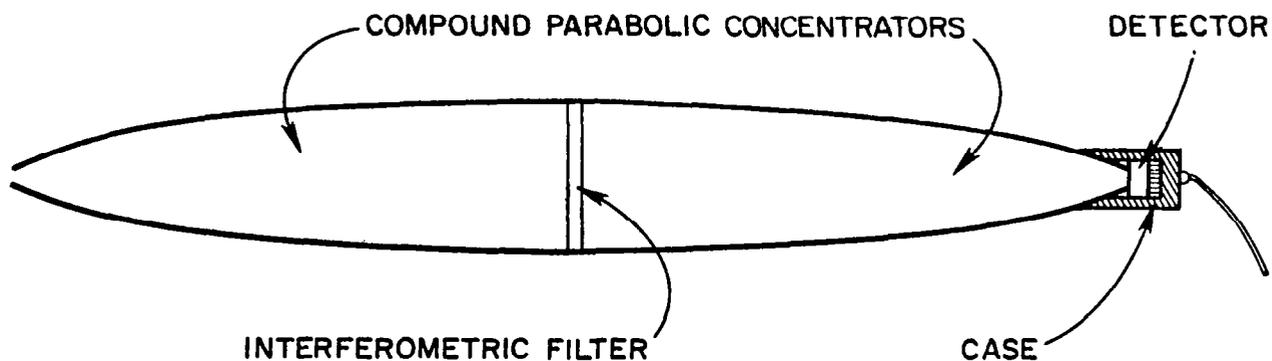
The laser beacon consists of two 5 mW He-Ne lasers, optics, and motor drive. The two lasers are placed underneath the beacon and brought to the top by means of prisms. Beam expansion optics are used to expand the beams for the cylindrical mirrors. These mirrors are used to reflect the expanded beams into the fan-shaped light beacon. The motor drive unit powers two orthogonal shafts in which these mirrors are mounted. The drive will rotate the mirrors giving sweep rate from two to four revolutions per second. A belt drive and flywheel are added for increased noise reduction from the motor.

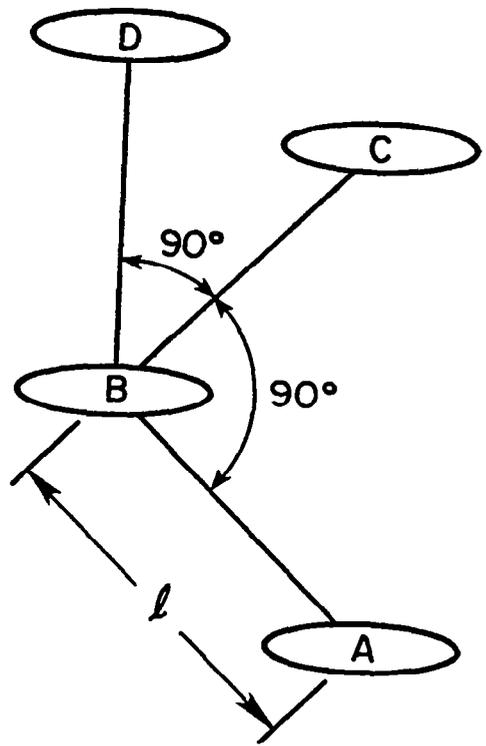
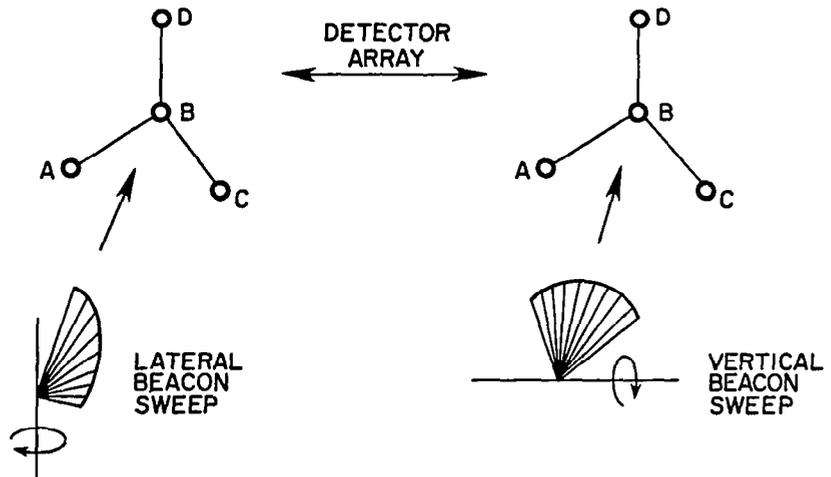
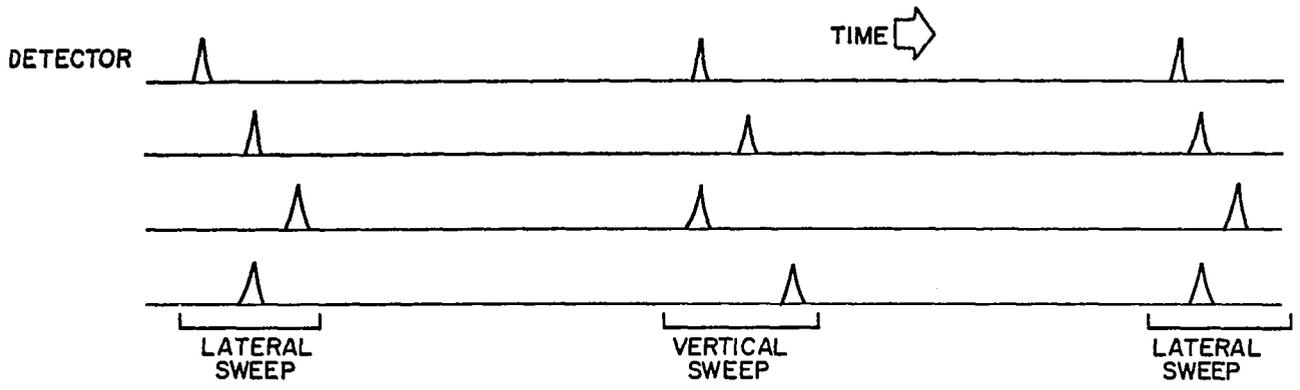




DETECTOR AND ARRAY SUBSYSTEM

The detectors are a pair of compound parabolic concentrators mounted end to end. This configuration results in a non-imaging wide-angle lens. A narrow-band interference filter is placed between the concentrators to reduce solar interference. A photodetector is placed at one end to collect the resulting light from a beam sweep. Further electronic filtering is done and is made compatible with our timing circuitry. The detector array that we are testing is a right tetrahedron of four detectors. This gives a simpler mathematical relation between the rotation axes of the beacon and the detector array.





MICROPROCESSOR SUBSYSTEMS

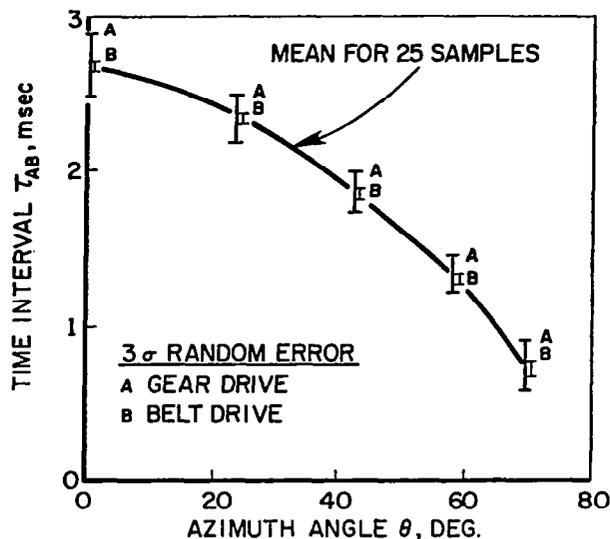
A microprocessor is used to implement the vector relations and to do further signal conditioning on board the detector-carrying aircraft. This computer is also transmitting the error signals to the helicopter, driving the I/O interface with the test engineer, and outputting the measurements to a data recording device. This system consists of a 4 MHz Z-80 microprocessor, a 9511 math chip for high speed floating point arithmetic, an 8253 counter/timer board for 0.5 microsecond timing resolution, and other peripheral drivers. A radio link is put into the system to transmit serial data from the aircraft to the helicopter. Another microprocessor is used in the helicopter for driving the displays. A glide slope indicator displays the Y-Z error measurement and a LED panel meter displays the X error measurement. This microprocessor will also have other warning lights and error checking functions.

TESTING

Static tests were run to examine system performance without aircraft dynamics. These tests were used to determine the current noise levels in the complete system. The following test results have been obtained:

- 1) A 1-foot standard deviation with approximately 100 feet beacon to detector array distance
- 2) A 1/2 degree standard deviation in angular measurements.

In these tests there was no signal conditioning done by the microprocessor.



FUTURE PLANS

With the conclusion of the static tests, a digital filter can be introduced into the software to improve system performance. Flight tests then will be run at NASA Ames Research Center for actual measurement capabilities. Further modifications then can be made to the hardware and software to meet or exceed the design specifications.

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